All About Sandboxes

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Mar 29, 2010

Abstract

Organizing design projects in a consistent way simplifies locating data, automating tasks, and reducing maintenance effort over time.

A sandbox is a defined directory structure containing a design and its associated files related to documentation, analysis, synthesis and simulation.

A sandbox can be a designer's personal copy of a design project or the actual project directory

Why Sandboxes

- You want to have a separate sandbox when you are experimenting with changes to a project or developing a piece of a project
- Version control systems such as cvs, subversion and Clearcase provide sandbox capability, but don't define what's in the sandbox
- Using a consistent directory structure simplifies locating data and design support files between projects and designers

How does Workspaces Desktop Fit?

- Workspaces Desktop supports creation of a “standard” directory structure and development of key scripts and documents that support the design in that directory structure
- Things you can do
  - Create the directory structure with default support files ready to support simulation
  - Create a Home Page for the project
  - Define parameters common to all projects
  - Create design documents that interact within that structure

Directory Structure for a Project

top_design_name – directory / project name

- doc – design documentation directory
- process – workflow files and tailored versions
- schematic – files relating to the design schematic
- sim – scripts and files relating to simulation
- source – design source code files
  - packages – subdirectory of special design packages
- synthesis – files relating to design synthesis (FPGAs)
- testbench – files relating to verification
  - packages – subdirectory of verification related packages

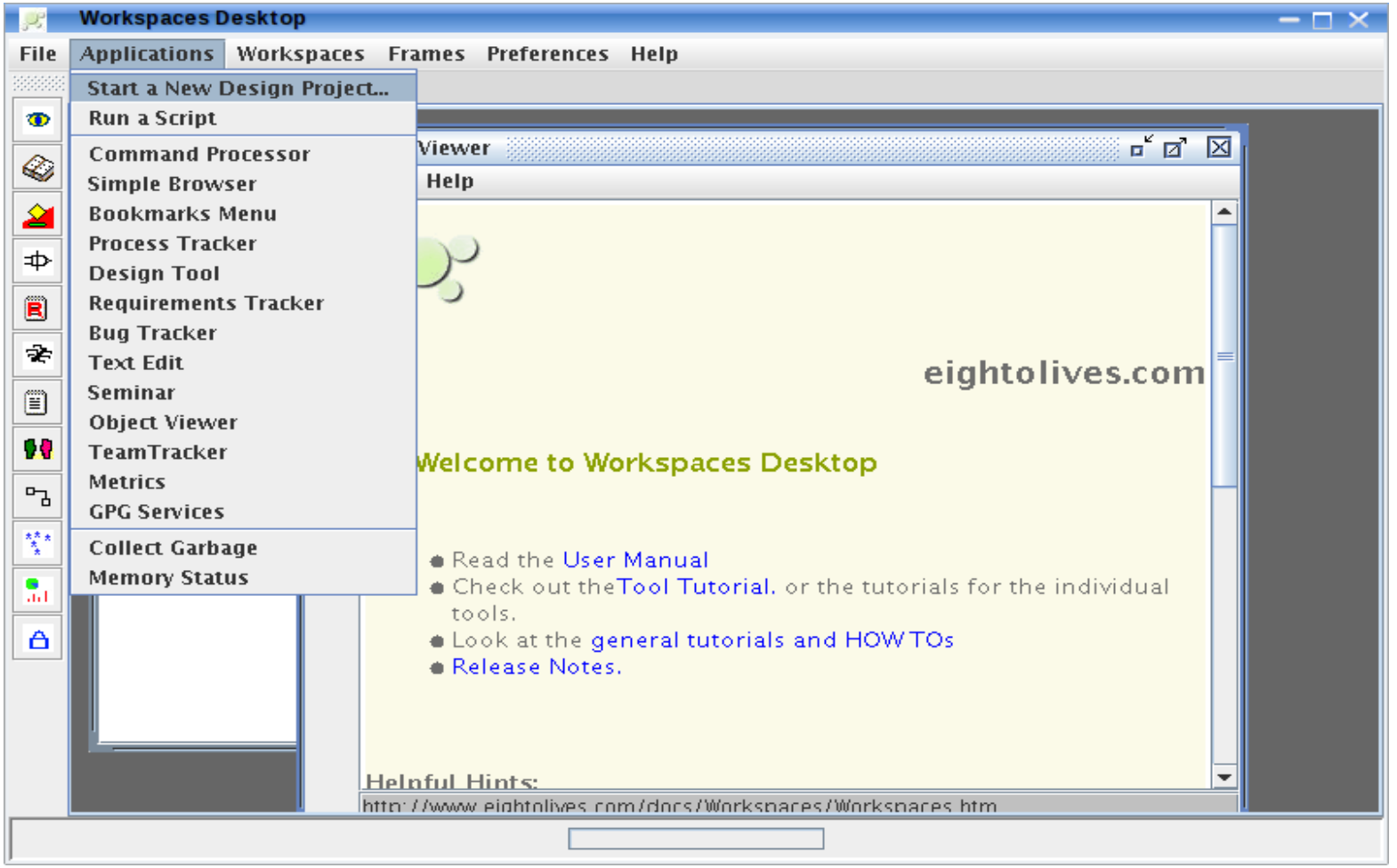
What's a Project file?

- A project file is an xml file located in the doc directory and named *project_name*_project.xml
- It defines pairs of Parameter Names and Parameter Values (similar to an .ini file)
- You use it to define the project directory names, links to key design files, links to documents, default parameters (like company name, file headers), tool personalizations
- Tools use this data to help automate and hyperlink

Let's say you have a VHDL file to simulate

- First, create a Sandbox
- Second, make any adjustments
- Third, simulate

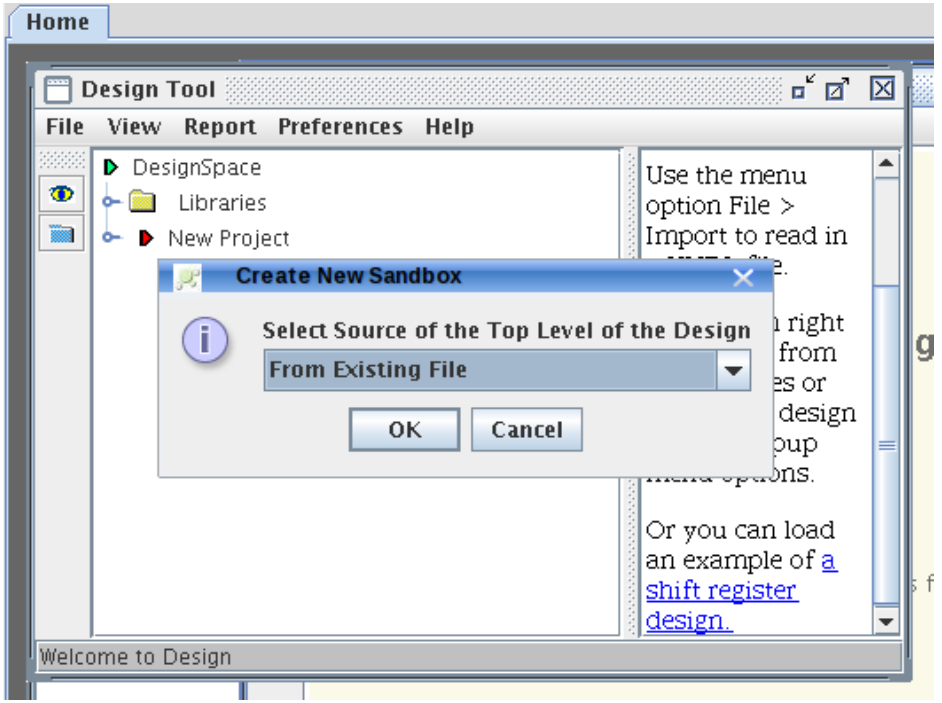
Step 1 Start the Sandbox Wizard

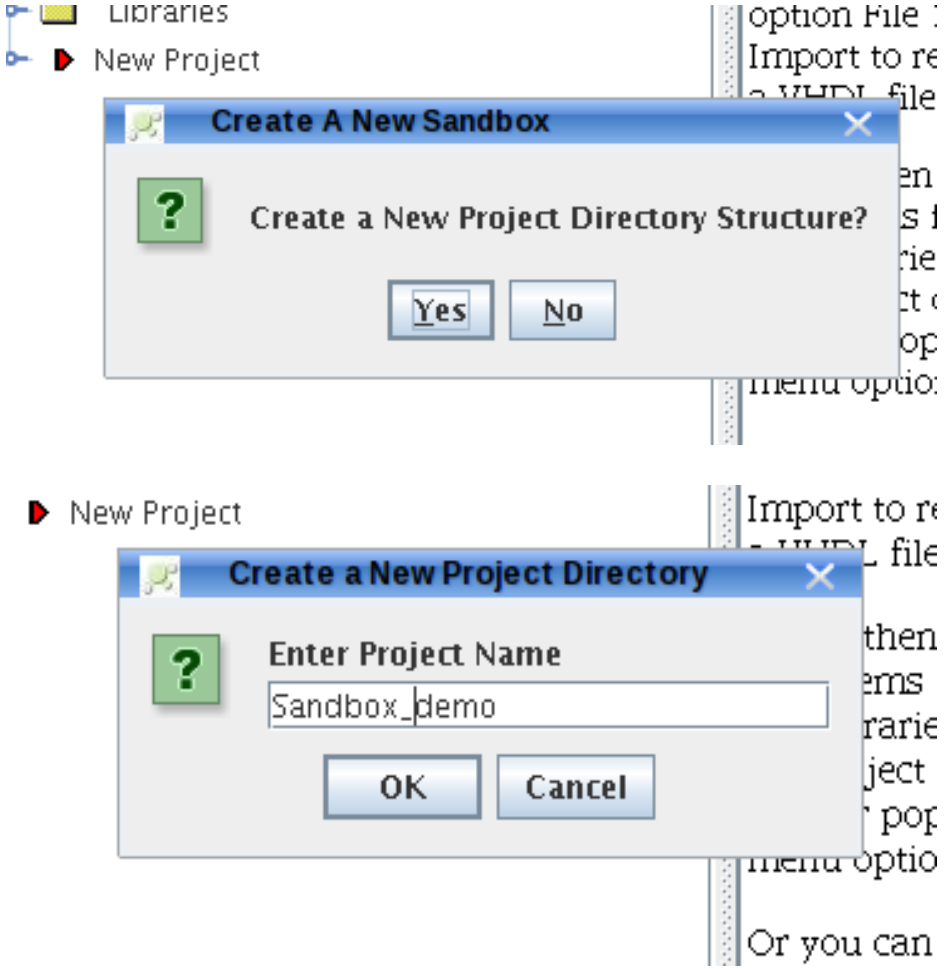


In Workspaces Desktop, select menu Applications > Start a New Design Project

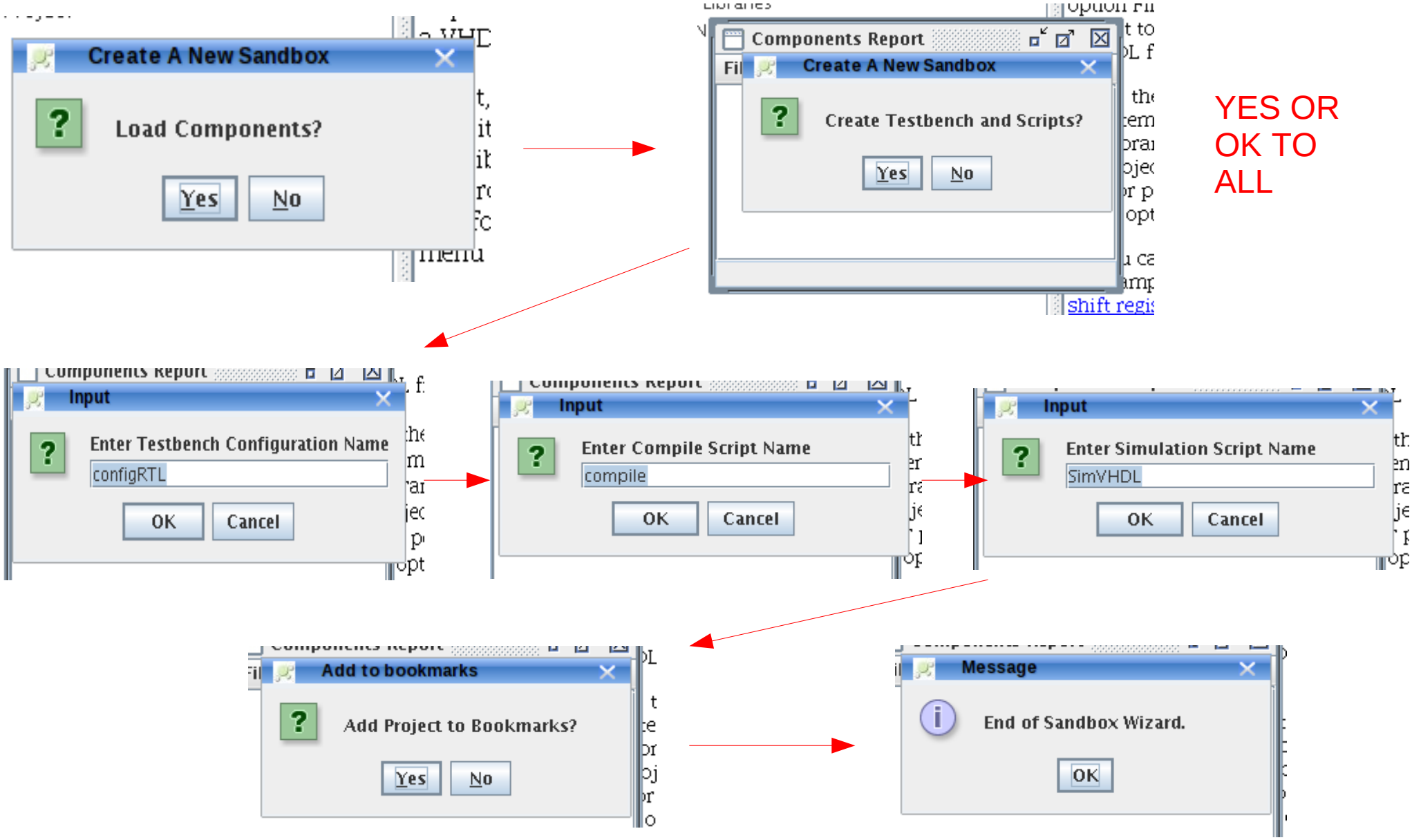
Respond to the Dialog Boxes

- A DesignTool window appears
- Select whether your top design is an existing file, a new design or a file already loaded into the DesignTool





- Click Yes to create a sandbox Directory Structure
- Give the project a name
- Select the directory where you want to put the Sandbox
- Then select the existing file you want to simulate



Resulting Directory Structure

Sandbox_demo:

doc/ process/ sim/ source/ synthesis/ testbench/

Sandbox_demo/doc:

Sandbox_demo_bugs.xml Sandbox_demo_project.htm
Sandbox_demo_teamtracker.xml

Sandbox_demo_metrics.xml Sandbox_demo_project.xml

Sandbox_demo/process:

Sandbox_demo/sim:

compile* modelsim.ini SimVHDL*

Sandbox_demo/source:

dff.vhd packages/

Sandbox_demo/source/packages:

Sandbox_demo/synthesis:

Sandbox_demo/testbench:

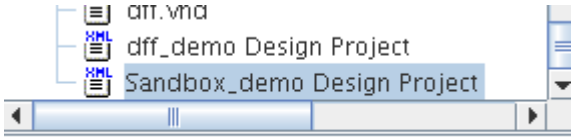
configRTL.vhd packages/ testbench_dff.vhd

Sandbox_demo/testbench/packages:

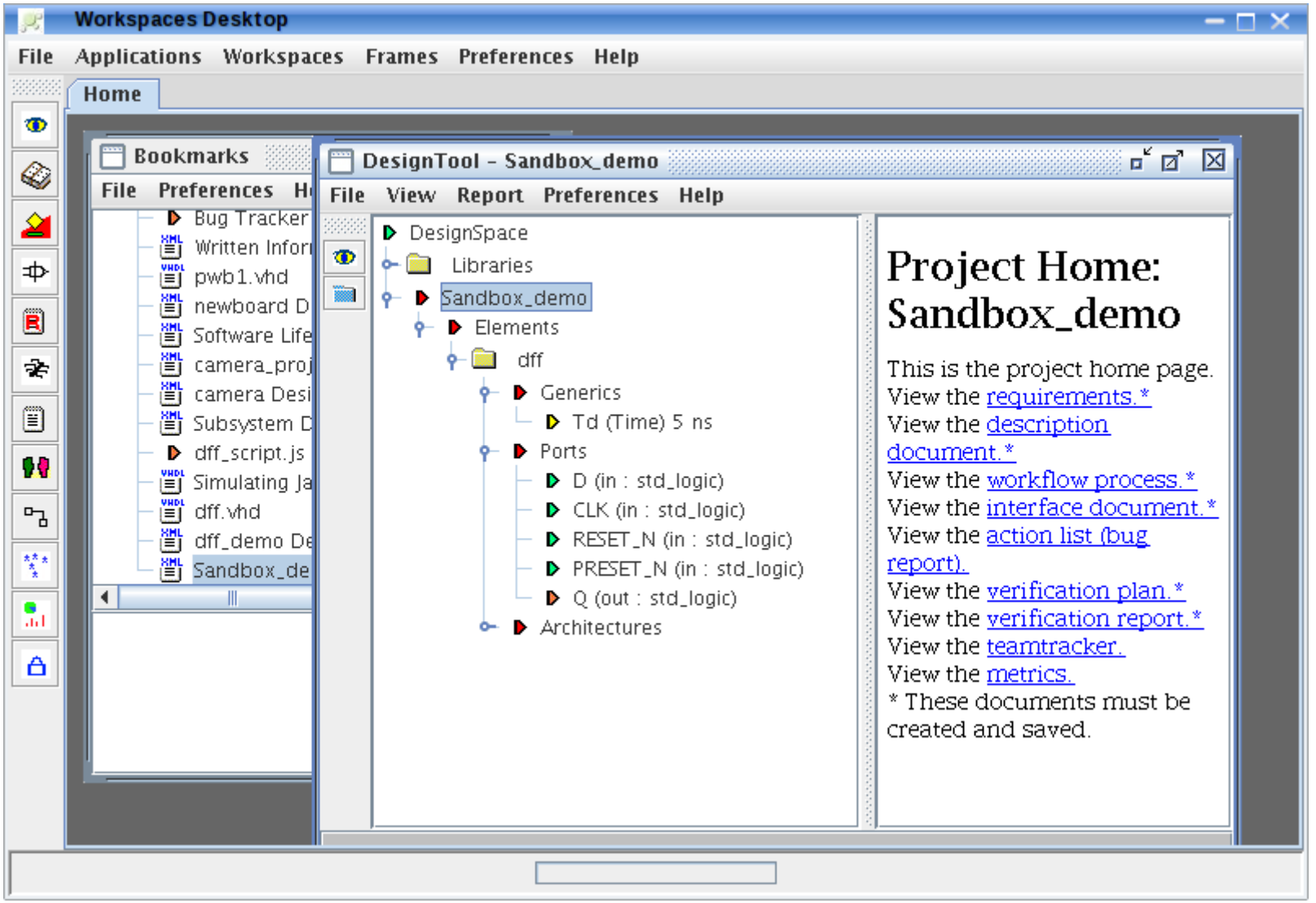
image_pb.vhd

The Sandbox is Ready

- Close The DesignTool window and any other reports
- Double click the project link that was added to the Bookmarks menu



- The DesignTool will open the project, display the HomePage, read in the top design and any other files you subsequently add to the project file



Notes

- The default scripts, compile and SimVHDL, are designed for use with the MentorGraphics Modelsim simulator. The corresponding default modelsim.ini file may need to be edited for your system environment. In Linux make sure these scripts are executable.
- If you use Windows OS, files compile.bat and SimVHDL.bat are created instead of the default ones for Linux

Notes

- The SimVHDL script simulates the configRTL VHDL file. You may need to modify the configRTL file if you have a non-trivial configuration
- The default testbench created by the DesignTool makes assumptions based on a signal name convention that may not be correct for your file. Check that reset, clocks and signal polarities are correctly represented.

Ready to Simulate

- The default testbench only provides a “Reset Test” and an “Output Enable Test” which may or may not be applicable to the design.
- Add your own “tests” and you're ready to roll

For more information

- Check the tutorials at http://www.eightolives.com/tutorials.htm
  - Workspaces Desktop Tool Overview
  - Simulating with ModelSim
- Read the Workspaces Desktop Users Manual