



Designing a Camera

A Demonstration Using Workspaces Desktop

William_Kaupinis@eightolives.com
March 16, 2010

Abstract

This presentation shows how to use the eightolives Workspaces Desktop and DesignTool to create a partially complete design of a digital camera.

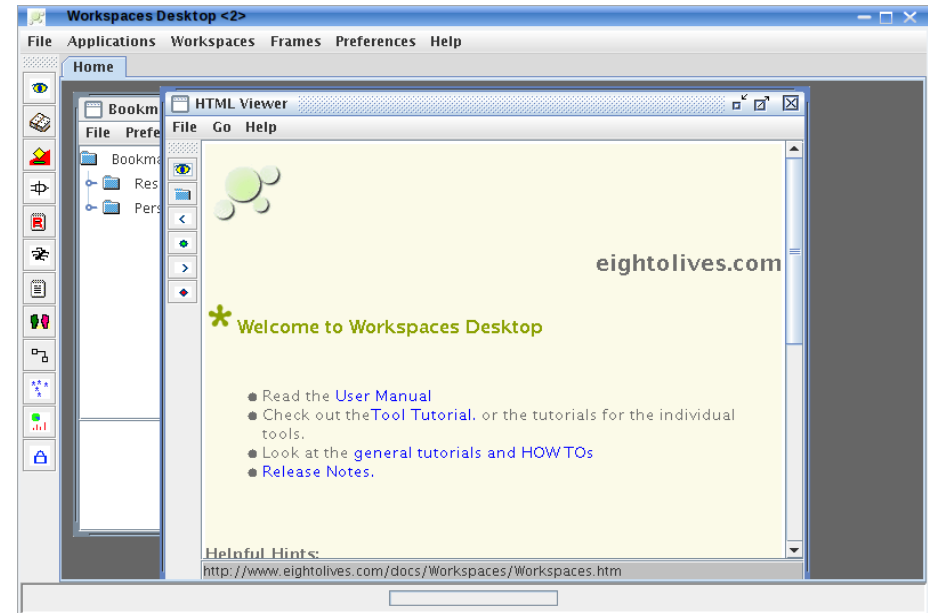
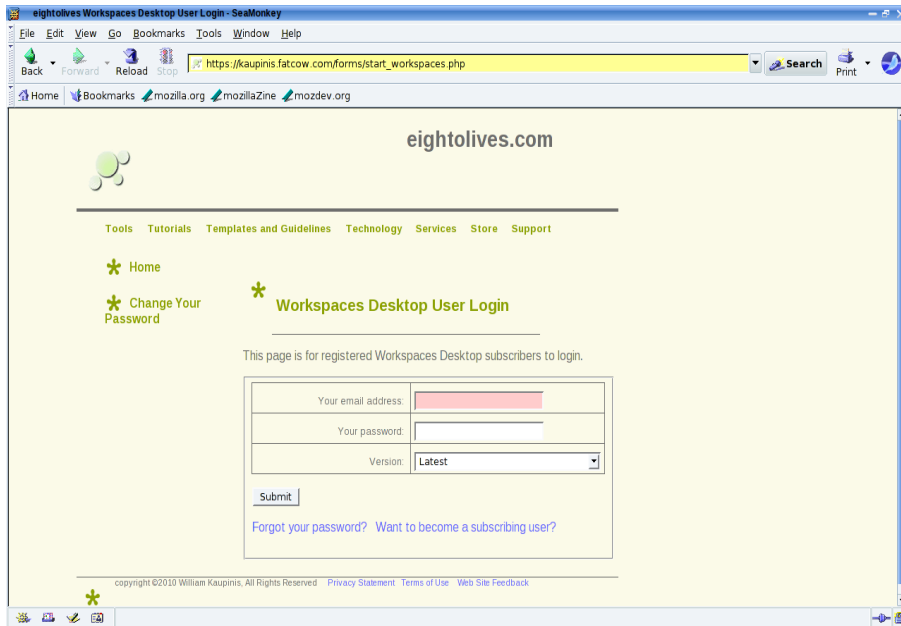
It demonstrates:

- Creation of a sandbox project
- Use of the DesignTool
- Expressing a concept using “real” and placeholder parts
- Performing design checks
- Creating a schematic
- Saving the design

Getting Started

- Workspaces Desktop is a development and analysis environment for digital designs
 - It includes various tools including DesignTool which is used to express and view a design
 - Java based so it runs wherever Oracle's Java runs
- You get a subscription (1 year) to the tool at <http://www.eightolives.com>
 - Start the tool from the web page and the latest version is downloaded for use
 - Libraries and help are available on-line

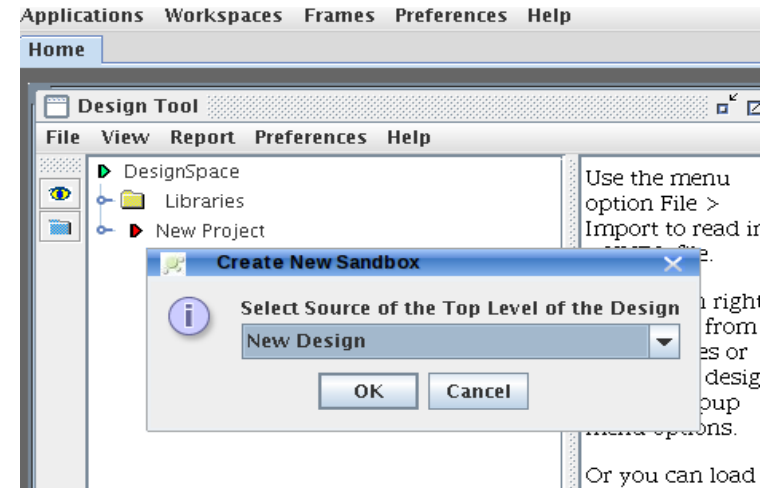
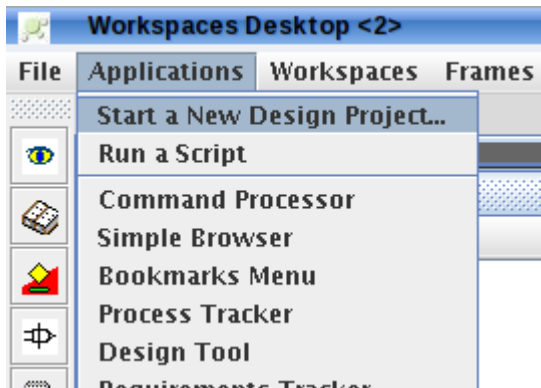
Log in & Workspaces Desktop Starts



- Your User Name is your email address
- An initial password is sent to you when you subscribe
- Change your password on-line

- The program is downloaded and started using Oracle's Java Web Start technology
- A "Welcome page" and the Bookmarks menu tree appear as default

Next, we create a design sandbox



- Select from the Main Menu: Applications > Start a New Design Project
- A DesignTool window will appear and a sequence of dialog windows guide you through the creation of a project sandbox.
- In the “Create A New Sandbox” window, select “New Design” then OK

Answer all the Sandbox Dialogs

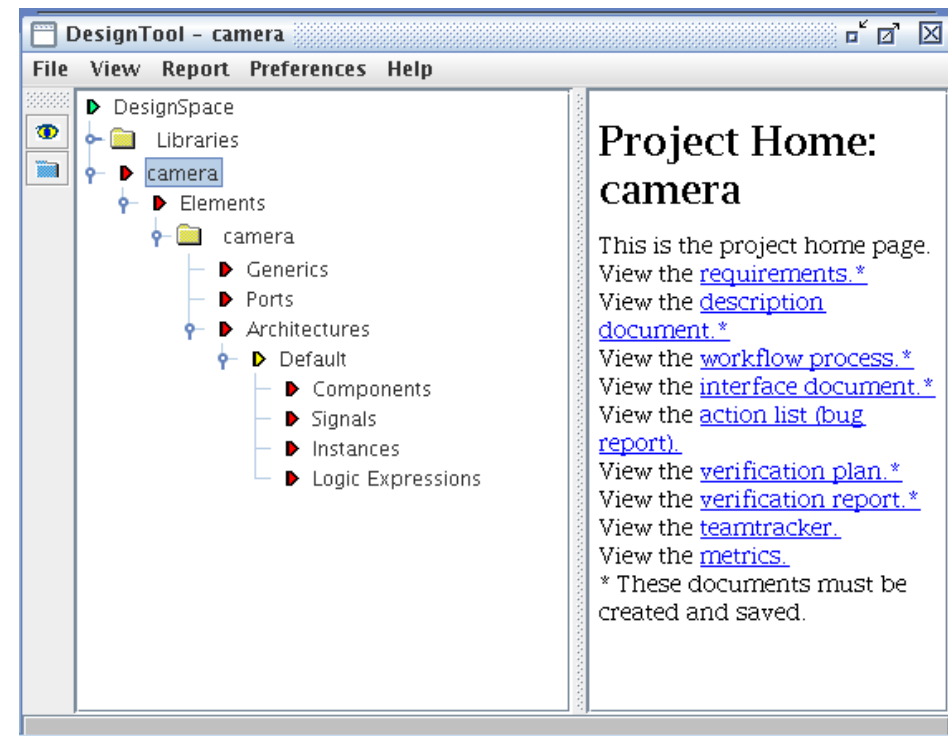
- Create A new Project Directory Structure – “Yes”
- Enter Project Name - “camera”
- Select a Destination Directory – select a directory where you want to put the project
- Enter New Design Top element Name - “camera”
- Add New Input Ports Now? - “No”
- Add New Output Ports Now? - “No”
- Add New INOUT Ports Now? - “No”
- Create Testbench and Scripts? - “Yes” (if you plan to use modelsim, doesn't hurt)
- Enter Testbench Configuration name - “configRTL” OK
- Enter Compile Script Name - “compile” OK
- Enter Simulation Script Name - “SimVHDL” OK
- Add Project to Bookmarks - “OK”

This sequence created the project directory “camera” at the selected destination along with key project files

Copyright © 2010 William Kaupinis All Rights Reserved

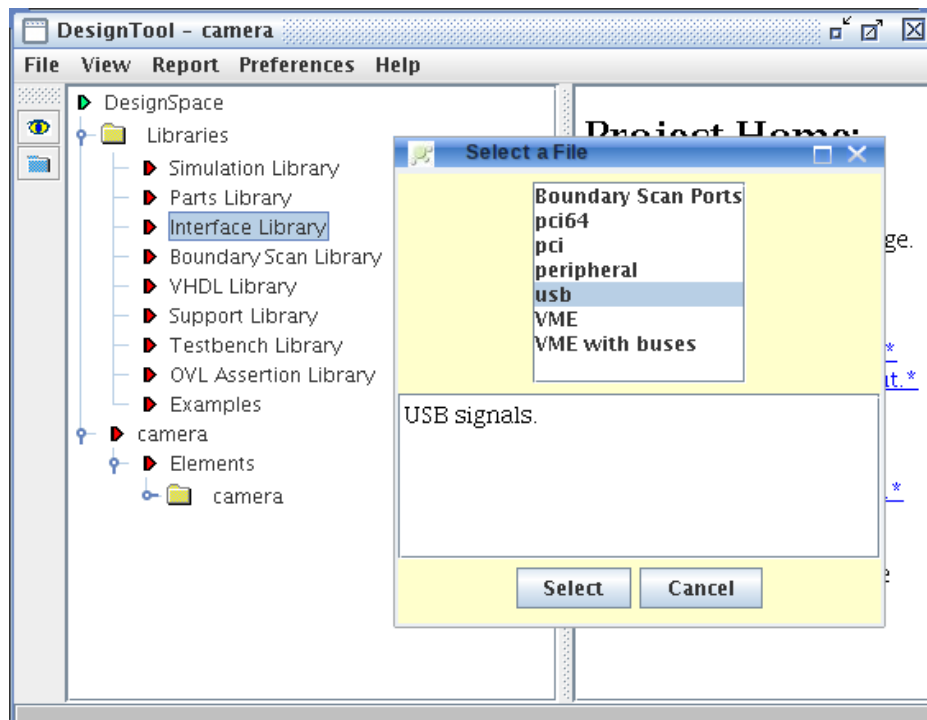
Open the Project from Bookmarks

- Close the current DesignTool windows
- In the Bookmarks tool, open the Personal folder and double click on the link “camera Design Project”



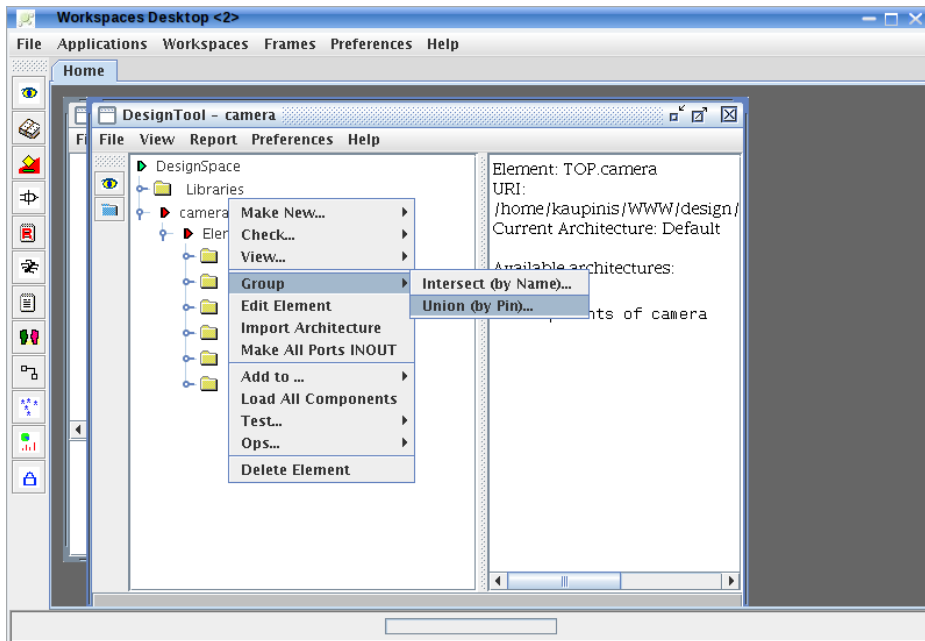
Selecting the Project in the left frame displays the Project Home Page in the right frame. Under Elements we see the top design Element “camera” and its structure

Pick Parts and Interfaces from the Libraries



- In the Libraries tree, right click Interface Library, Load Element from Library and select “usb”
- Repeat, selecting “Boundary Scan Ports”
- In Parts Library select MT9M001
- Repeat, selecting Resistor
- In Simulation Library select Clock Generator

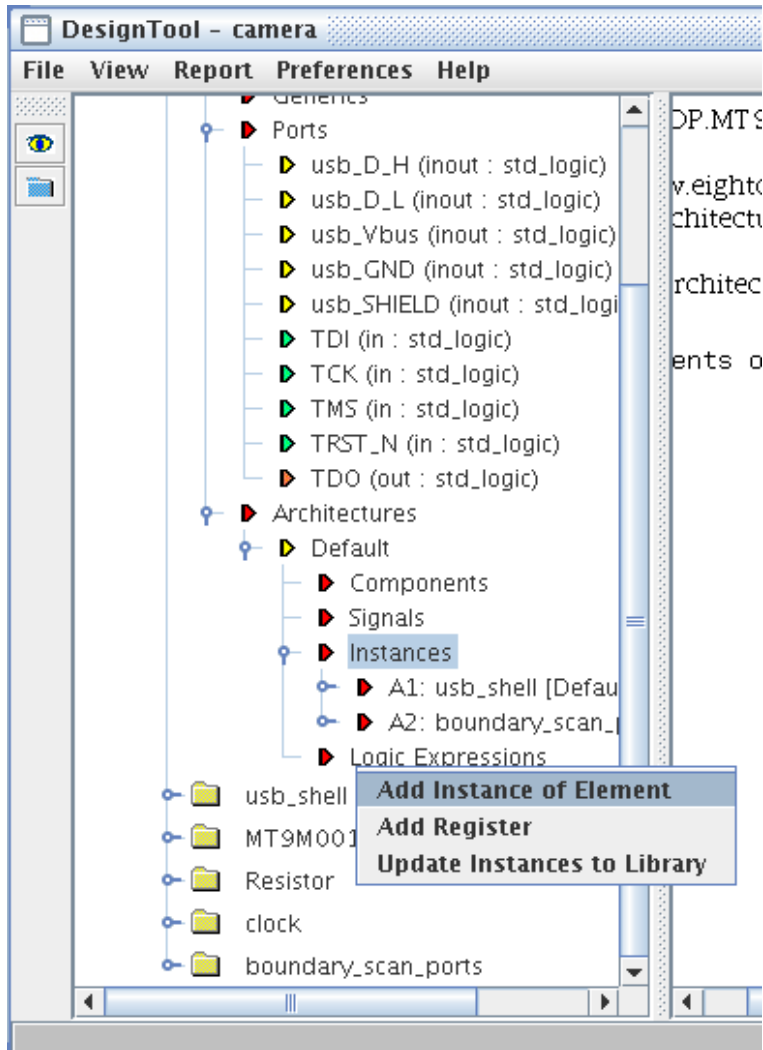
Group the Interfaces to Camera



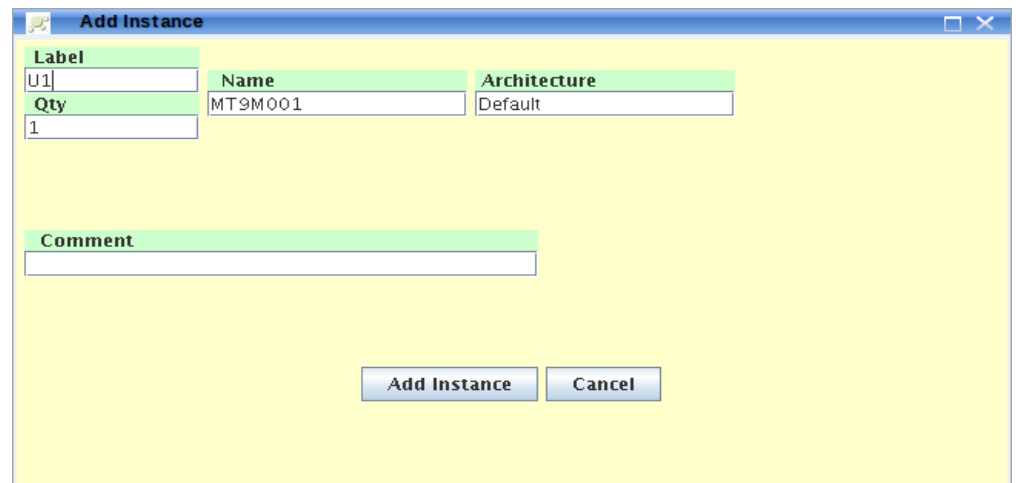
- First left click on usb_shell
- Then left click then right click camera
- Select Group > Union and assign label as “A1”
- Repeat process starting with boundary_scan_ports assigning label as “A2”

Group Union causes the first selected item to be added to the second item. This includes I/O ports. This allows us to add interfaces easily. The two blocks, A1 and A2, will be instantiated into camera, but we will replace them with an FPGA later.

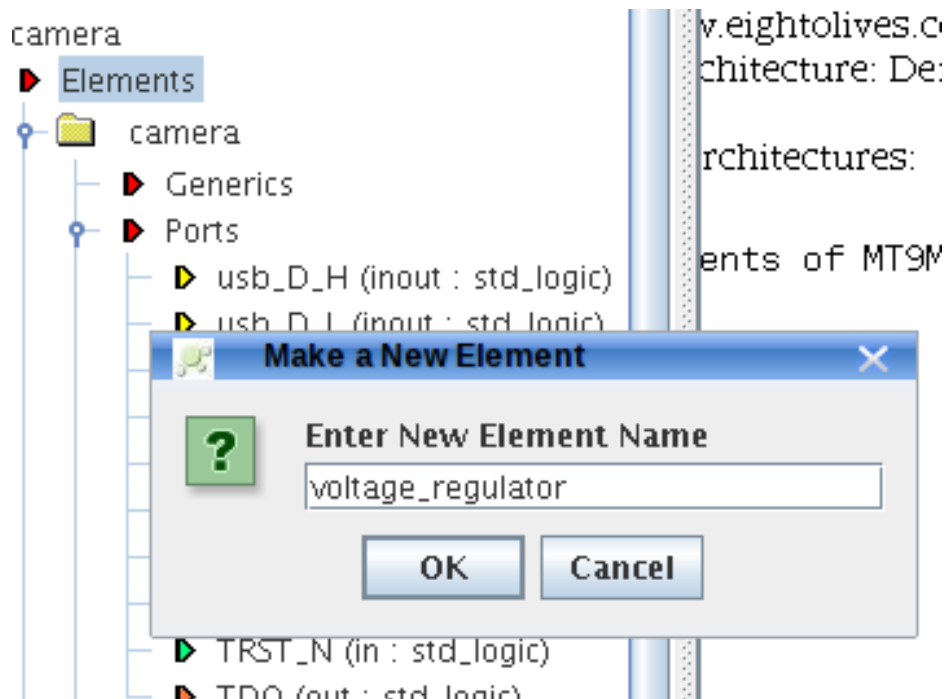
Instantiate Some Parts



- First left click MT9M001
- Then in camera > Architectures > Default, left click Instances then right click. Select Add Instance of Element. Enter label of "U1"



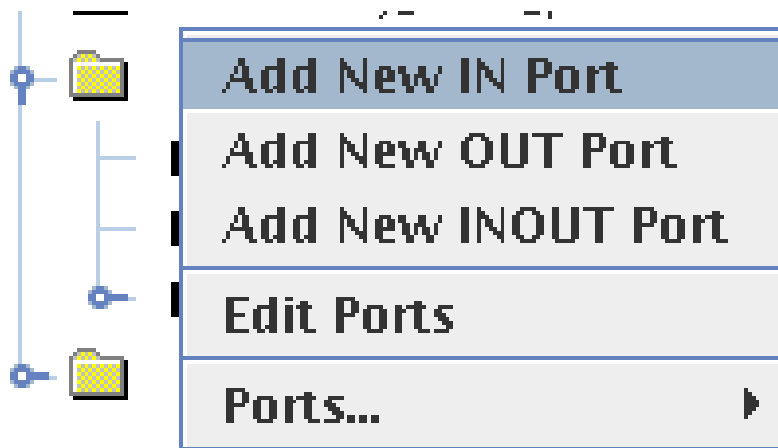
Create New Elements



- We need to create a voltage regulator and an FPGA
- Left click then Right click Elements
 - Select Add New Element
 - Enter new Element Name - “voltage_regulator”
 - Enter new Element Name - “camera_fpga”

Elements > Add New Element lets you define additional parts

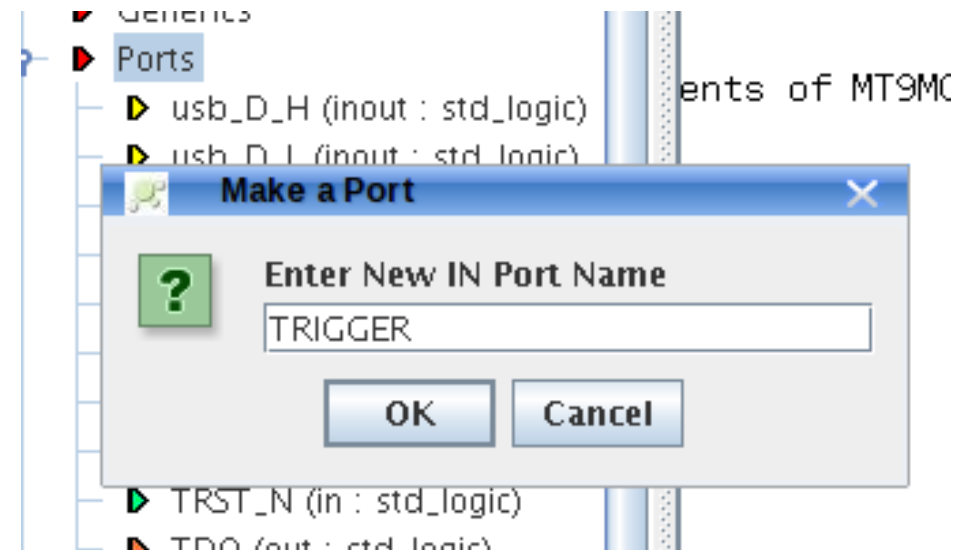
Add Some I/Os the Parts



- In voltage_regulator, left click Ports then Right click. Select “Add New IN Port”
- Add IN ports VDD, GND
- Using “Add New Out Port”, add OUT Port “VOUT”

Add Additional Top Level IO Ports

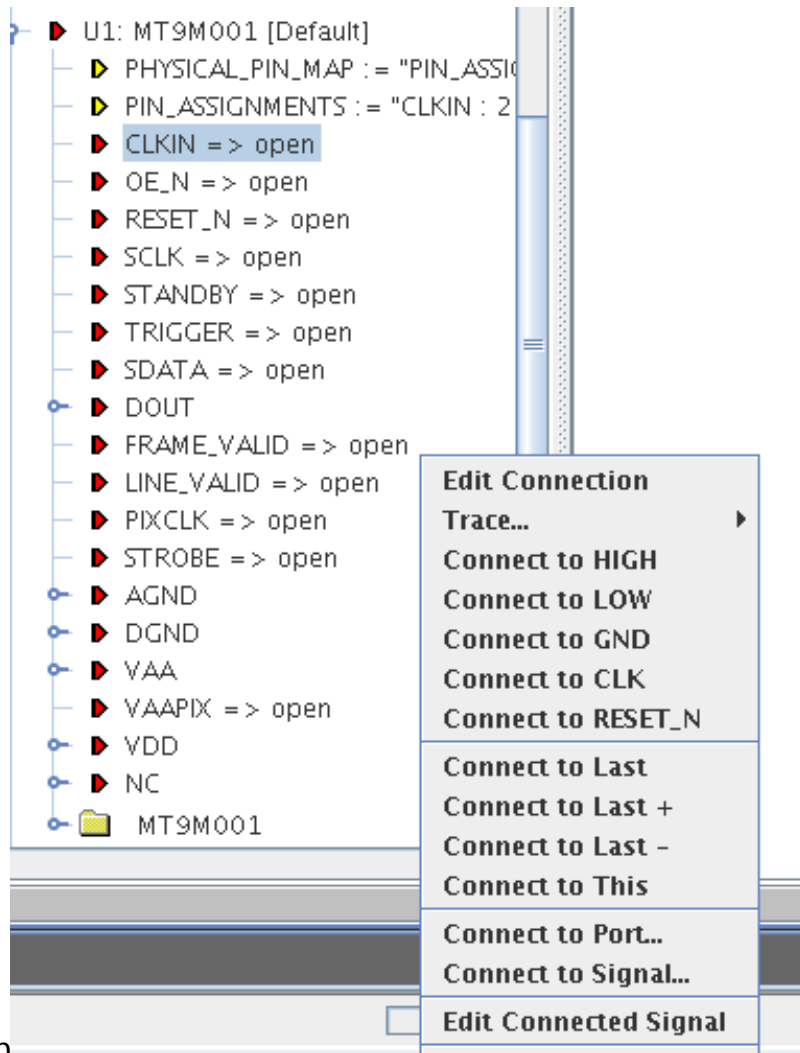
- In camera, left click Ports then Right click. Select Add a New IN Port
- Add IN ports TRIGGER, VDD, GND



Instantiate More Parts

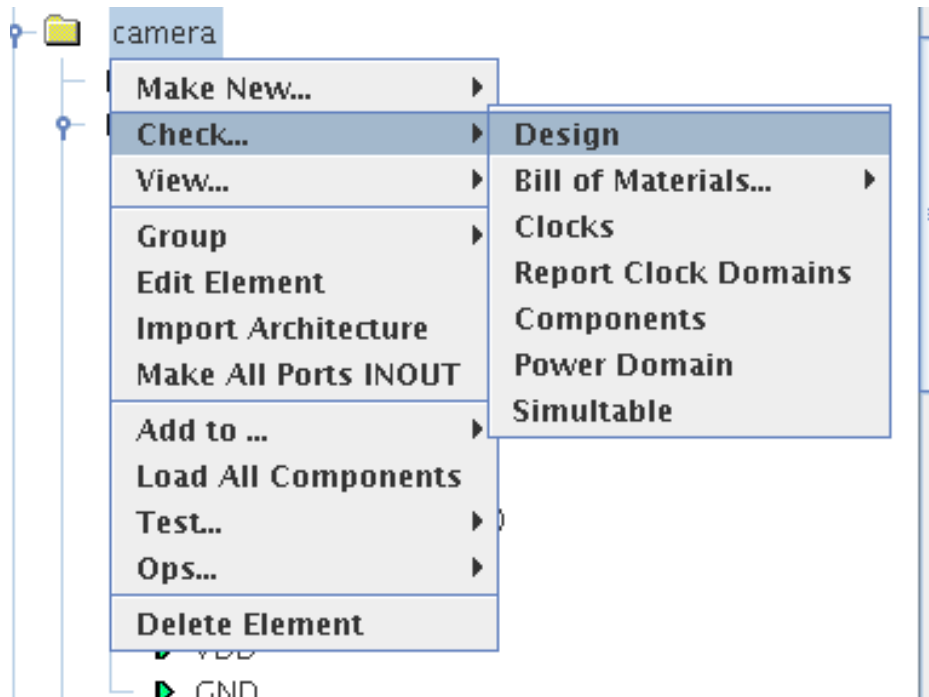
- Using the Instantiation method previously shown
 - Add voltage_regualtor, camera_fpga, and clock using labels U2, U3, U4
 - Add Resistor using label R1
 - Add another resistor using label R2

Connect the Pins to Signals and Ports



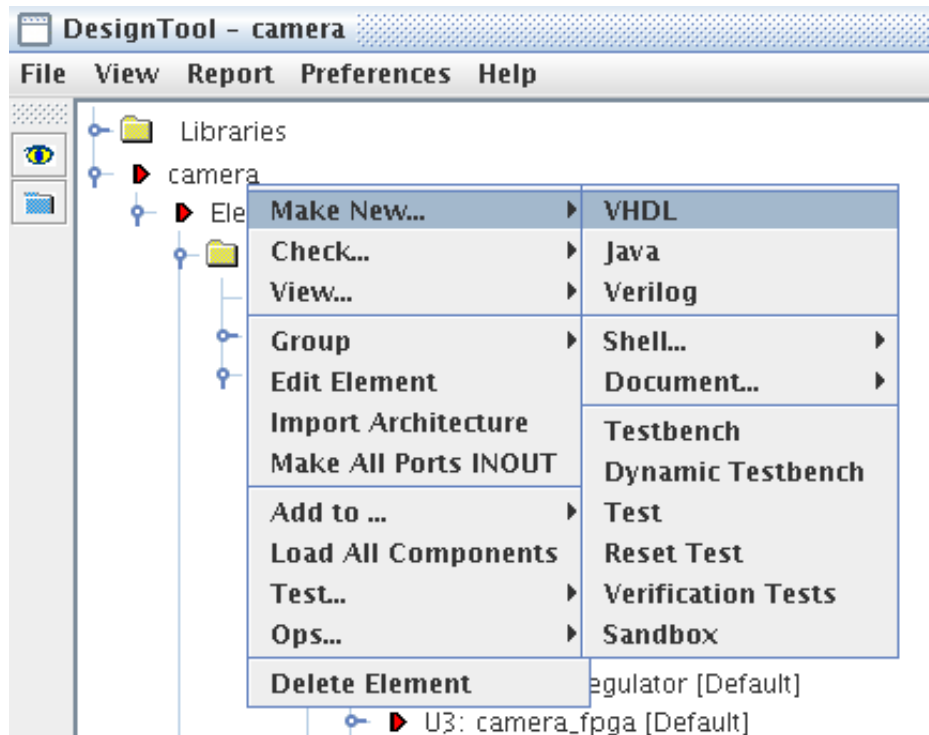
- For each instance in camera, right click each port and connect it appropriately.
- “Connect to This” connects to a signal of the same name
- “Connect to Port” gives you a popup list of Ports to select from
- “Connect to Signal” gives you a popup list of Signals to select from
- Edit connection lets you create a new Signal to connect to

Check your design



- Right click camera, Check > Design provides a report of unconnected signals, questionable connections

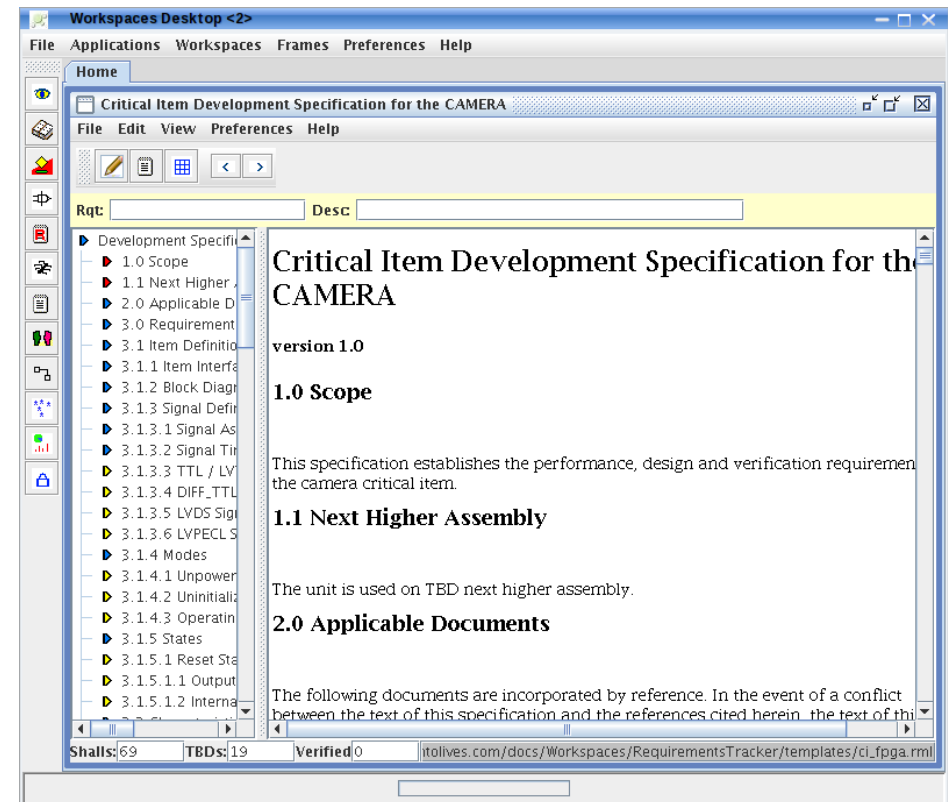
Save your design as VHDL



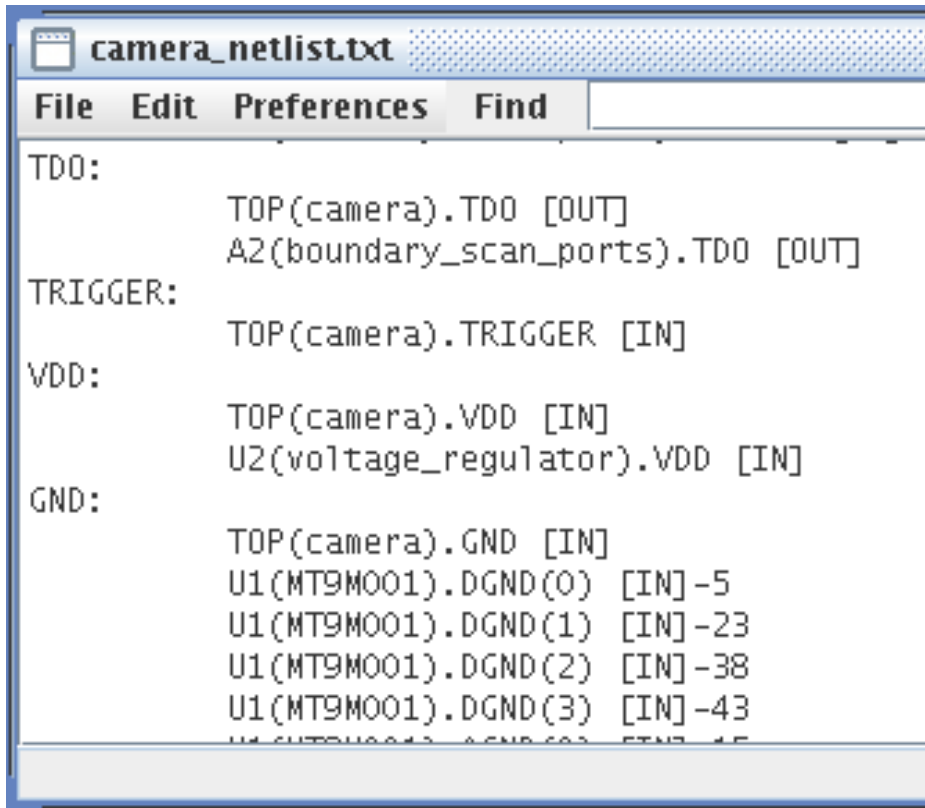
- Right click camera, Make New > VHDL creates the VHDL code for the design
- The code appears in an Editor window.
- File > Save As select camera.vhd

Create Documentation

- Right click camera, Make New > Make New > Document > Requirements Document generates a partially filled-in template of a specification that you can edit in the RequirementsTracker tool.



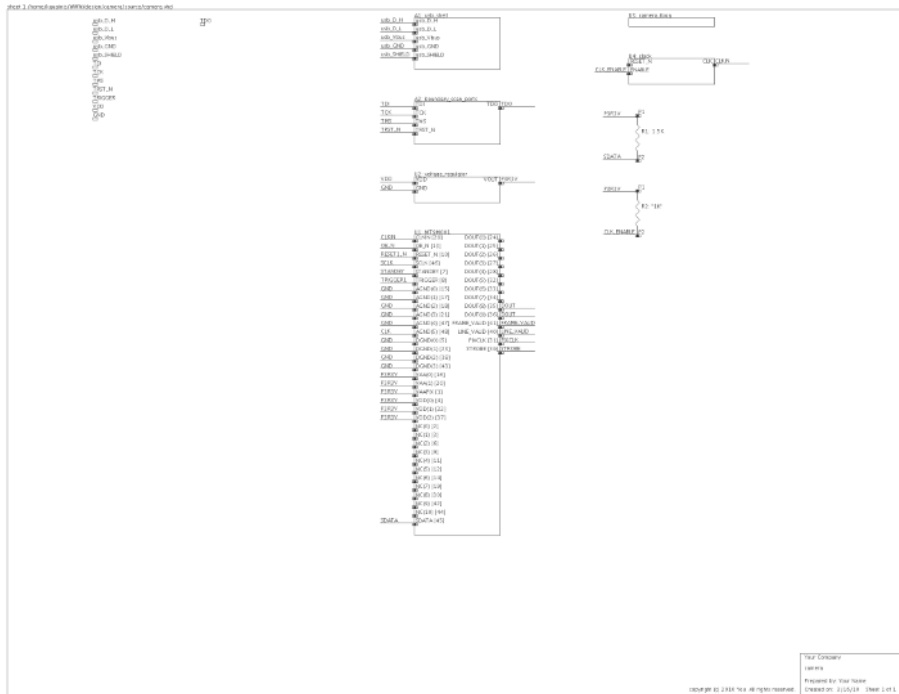
Make a Net List



```
camera_netlist.txt
File Edit Preferences Find
TDO:
    TOP(camera).TDO [OUT]
    A2(boundary_scan_ports).TDO [OUT]
TRIGGER:
    TOP(camera).TRIGGER [IN]
VDD:
    TOP(camera).VDD [IN]
    U2(voltage_regulator).VDD [IN]
GND:
    TOP(camera).GND [IN]
    U1(MT9M001).DGND(0) [IN] -5
    U1(MT9M001).DGND(1) [IN] -23
    U1(MT9M001).DGND(2) [IN] -38
    U1(MT9M001).DGND(3) [IN] -43
    U1(MT9M001).DGND(4) [IN] -45
```

- Right clicking camera's architecture Default gives you the option to create a net list

Create a Schematic



- Right click camera, View > Schematic displays an automatically generated schematic in the ObjectViewer tool.

Summary

- Although all the design details haven't been filled in, the methods of assembling the framework of a design has been demonstrated.
- The demonstration mixed library models with generated models, demonstrated interconnection and showed aspects of editing a design.
- This project is viewable on-line from the DesignTool's Getting Started window.