Modifying SDF Files For Min, Typ, Max Timing

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Abstract

This presentation explains how to create an SDF file that can be used to perform minimum timing simulations for FPGAs.

Newer FPGA implementation tools create back-annotation SDF files with maximum timing numbers only.

Min timing simulations can unveil hold time issues

Min timing simulations are needed if module test vectors are to be generated

Approach Applies Scale Factors

This method scales the max timing numbers to create an SDF file with min/typ/max triplets

Scaling is based on historic delay annotation factors for CMOS

- Voltage Variation
- Temperature Variation
- Process Variation

	Condition	Min Factor	Typ Factor	Max Factor
Temperature Factor	-55C to +125C	0.7	1.0	1.4
Voltage Factor	+/- 10%	0.8	1.0	1.2
Process Factor	constant	1.4	1.0	1.4
Total Factor (TF)		0.8	1.0	2.4
TF max normalized		0.3	0.4	1.0

The Steps

- Generate the normal max timing SDF file using the synthesis/place & route tool
- Post-process the max SDF file using the Workspaces Desktop's DesignTool
- Save the new SDF file with a different name

Post-processing SDF Files

File > Open your SDF file

The Set SDF Delay Ratios window will pop up. Recommend using the defaults.

Click the Update SDF Button and save the data to a new file name.