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### Getting Pin Numbers On a Design

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# eightolives.com Abstract

A design's pin number information is not typically recorded in a consistent manner.

Saving pin number information in a VHDL source file provides a way to address this issue.

The eightolives Workspaces Desktop DesignTool has features to help capture and manage pin information.

# eightolives.com The Problem

- Different FPGA vendors specify device pinouts using different proprietary constraint file formats (i.e. .ucf files)
- Tools that translate circuit card schematics to VHDL don't capture the pin information.

# eightolives.com Proposed Solution

- Capture pin information in the design's top level VHDL file using the format prescribed for Boundary Scan Descriptions (IEEE 1149.1)
  - FPGA vendors provide BSDL files for their various packages
  - Schematics saved as EDIF files contain pin information
  - Use the eightolives Workspaces Desktop tool to help integrate this information and create the VHDL file

### **eightolives.com** Extract from Texas Instruments SN74LVTH18502ALS BSDL File

entity sn74lvth18502a is

generic (PHYSICAL\_PIN\_MAP : string := "UNDEFINED");

port (OEAB\_NEG1:in bit;

OEAB\_NEG2:in bit;

OEBA\_NEG1:in bit;

.....

use STD\_1149\_1\_1990.all; -- Get standard attributes and definitions

attribute PIN\_MAP of sn74lvth18502a : entity is PHYSICAL\_PIN\_MAP;

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constant PM : PIN\_MAP\_STRING := "OEAB\_NEG1:62, OEAB\_NEG2:21,"&

"OEBA\_NEG1:53, OEBA\_NEG2:30,"&

"LEAB1:60, LEAB2:22, LEBA1:54, LEBA2:28,"&

"CLKAB1:59, CLKAB2:23, CLKBA1:55, CLKBA2:27,"&

"A1:(63,64,1,2,3,5,6,7,8),"&

"A2:(10,11,12,14,15,16,17,18,19),"&

"B2:(51,50,49,48,46,45,44,43,42),"&

"GND:(6,13,23,30,40,47,57,64),"&

"VCC:(2,19,36,53),"&

"NC:(1,18,35,52),"&

"TCK:37, TDI:34, TMS:68, TDO:3 ";

The pin information is contained in a VHDL String listing signal name and pin number

## **eightolives.com** How does Workspaces Desktop Help?

- Top level Port names of an FPGA design don't match the Port names used in the BSDL file
  - Workspaces Desktop captures pin data from BSDL, ucf and edf files
  - Workspaces Desktop can merge pin and port data using menu commands
    - Group Intersect by Name (design file and constraint file)
    - Group Union by Pin (design file and BSDL file)
- There may be no electronic source of pin information so you have to specify it manually
  - Edit Ports window is a table for manual pin entry

### eightolives.com

To manually add Pin Numbers, first read in your design file



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## eightolives.com Fill in the Pin column

R	Edit Ports								×
File	Operations	Preferences							
	Port Name	Pin	Mode	Туре	At Reset	Is Clock	Domain	Setup	
CLK		2	IN	std_logic		true			-
CLR_N	1	1	IN	std_logic			ASYNC		
Ρ		7	IN	std_logic			CLK		
Т		10	IN	std_logic			CLK		
LD_N		9	IN	std_logic			CLK		
A		3	IN	std_logic			CLK		
В		4	IN	std_logic			CLK		
С		5	IN	std_logic			CLK		
D		6	IN	std_logic			CLK		
QA		14	OUT	std_logic	'0'		CLK		
QB		13	OUT	std_logic	'0'		CLK		
QC		12	OUT	std_logic	'0'		CLK		
QD		11	OUT	std_logic	'0'		CLK		
CY		15	OUT	std_logic	'0'		CLK		
									-
•									
Delete Rows Updated Ports Cancel									

Then click the Updated Ports button.

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## eightolives.com Make the VHDL file

#### Right click the top Element and select Make New > VHDL

🛅 Design Tool							
File	View	Report	Preferences	Help			
	▶ Des ► 🚞	ignSpace Libraries				Element: URI:	count1
	<b>∲</b> - ▶	New Proje	Make New.		Þ	VHDL	ar Ar
	<b>9</b> −	Elemei	Check		۲	Java	ec
			View		•	Verilog	
			Group		•	Javascript	• it€
			Edit Elemer	it		Shell	•
		-	Import Arch	nitecture		Document	▶ ati
			Make All Po	orts INOUT		Testbench	tľ
						в : т. н	

The entity of the VHDL file will include the pin information.

ENTITY count161 IS

"QD : 11," & "CY : 15";

END count161;

```
GENERIC(
     Τd
          : Time := 2 ns;
    PHYSICAL PIN MAP : String := "PKG PINS"
     );
PORT (
            : IN std logic; -- rising edge clock
     CLK
  . . . . .
    СҮ
          : OUT std logic
                              -- carry out
    );
SUBTYPE PIN_MAP_STRING IS STRING;
CONSTANT PKG PINS : PIN MAP STRING :=
"CLK : 2," &
"CLR N : 1," &
"P: 7," &
"T : 10," &
"LD N : 9," &
"A : 3," &
"B: 4," &
"C: 5," &
"D:6," &
"QA : 14," &
"QB : 13," &
"QC : 12," &
```

## eightolives.com For FPGAs you can import .ucf data

- First read in the design: File > Import File
- Then read the FPGA's ucf file that has pin numbers included: File > Import File
- Select (left click) the ucf Element then select the top FPGA Element
- Right click and select Group > Intersect (by Name)
- Click the Intersect button in the pop-up dialog



#### The pin number information will now be transferred to the FPGA design

## eightolives.com To add the other package pins...

- To add the unused, power, ground and dedicated pins to the design
  - File > Import the vendor's BSDL file
    - Respond YES to Convert Bit to Std\_Logic dialog
  - Select (left click) the BSDL Element
  - Left then right click the FPGA Element and select Group > Union (by pin)
    - This adds the remaining package pins to the design
    - A side effect is that it adds an instance of the BSDL
       Element to the design, but you can select that Instance and Delete it.

### eightolives.com or... put the FPGA in the BSDL package

👕 DesignTool - pin_demo		👷 Add Instand	e		
File View Report Preferences Help		Label			
<ul> <li>DesignSpace</li> <li>Libraries</li> <li>pin_demo</li> <li>Elements</li> <li>fpga_a</li> <li>fpga_a_ucf</li> <li>XC2S100E_FT256</li> <li>Generics</li> <li>Ports</li> <li>Architectures</li> <li>Co Add Instance of Eler</li> <li>Sig Add Register</li> </ul>	Elemer URI: /home Currer. Availal Defaul Bound Con fpg	U1 Qty 1 Comment	Name fpga_a	Architecture shell Add Instance Cancel	
Logic Expressions					

- In the BSDL tree, right click the Default Architecture and select Use This Architecture
- Left click the FPGA Element then right click Instances within the BSDL tree
- Select Add Instance of Element and in the pop-up window add the label "U1"
- Click the Add Instance button

# eightolives.com Now we connect U1



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- Right click the instance U1 and select Connect to Parent by Pin
- The FPGA will now be connected to the BSDL top Element.
- Right click the BSDL
   Element and select
   Make New > VHDL

Save it.

### eightolives.com End result: FPGA connected to BSDL package



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	<u>U1: fpqa_a</u>
<u>10_H2</u>	ADC_CLKIN [H2]
<u>10_C5</u>	ADC_CONVST_N [C5]
<u>10_A4</u>	ADC_CS_N [A4]
<u>IO_N15</u>	ADC_D0 [N15]
<u>IO_N16</u>	ADC_D1 [N16]
<u>10_P7</u>	ADC_D10 [P7]
<u>10_N5</u>	ADC_D11 [N5]
<u>IO_P5</u>	ADC_D12 [P5]
<u>10_T3</u>	ADC_D13 [T3]
<u>10_R6</u>	ADC_D2 [R6]
<u>10_T6</u>	ADC_D3 [T6]
<u>10_P6</u>	ADC_D4 [P6]
<u>IO_M6</u>	ADC_D5 [M6]
<u>10_N7</u>	ADC_D6 [N7]
<u>10_R5</u>	ADC_D7 [R5]
<u>10_T5</u>	ADC_D8 [T5]
<u>10_R7</u>	ADC_D9 [R7]
<u>IO_P16</u>	ADC_EOC_N [P16]
<u>10_C1</u>	ADC_RD_N [C1]
<u>10_H3</u>	ADC_STBY_N [H3]
<u>10_D8</u>	CLK5M [D8]
<u>10_A9</u>	CPU_A0 [A9]
<u>10_89</u>	CPU_A1 [B9]
<u>10_A8</u>	CPU_A2 [A8]
<u>IO_R14</u>	CPU_A3 [R14]
<u>IO_F14</u>	CPU_A4 [F14]
<u>IO_P8</u>	CPU_A5 [P8]
<u>10_T7</u>	CPU_A6 [T7]
<u>IO_M11</u>	CPU_A7 [M11]

# eightolives.com VHDL generated from eightolives' Schematic

- A schematic normally uses component symbols that have pin numbers assigned.
- Generating VHDL using eightolives' Schematic will add two generics to an instantiated component:
  - PHYSICAL\_PIN\_MAP : STRING := "PKG\_PINS";
    - This defines which package to use. Other example: "SOP16"
  - PKG\_PINS : PIN\_MAP\_STRING := "CLK : 4, CLK\_N : 5, GND : 3," & "NC : 1, OE : 2, SCL : 8, SDA : 7,VDD : 6";
    - This defines the pin name : pin number pairs

# eightolives.com For more information

- Check the tutorials at: http://www.eightolives.com/tutorials.htm
  - Workspaces Desktop Tool Overview
- Checkout the VHDL resources links at: http://www.eightolives.com/technology.htm
- Read the Workspaces Desktop Users Manual