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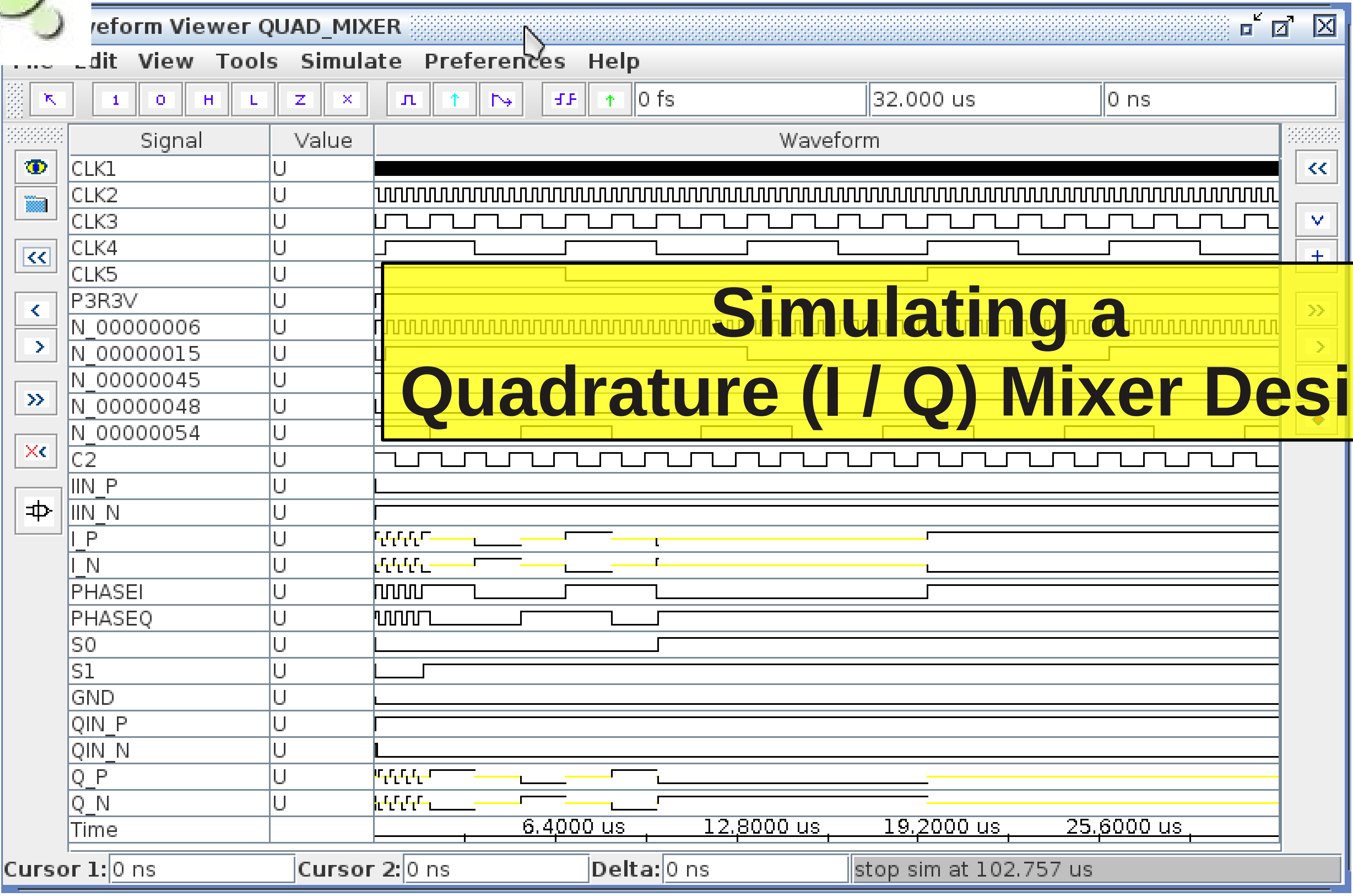

Simulating a Quadrature (I / Q) Mixer Design

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Abstract

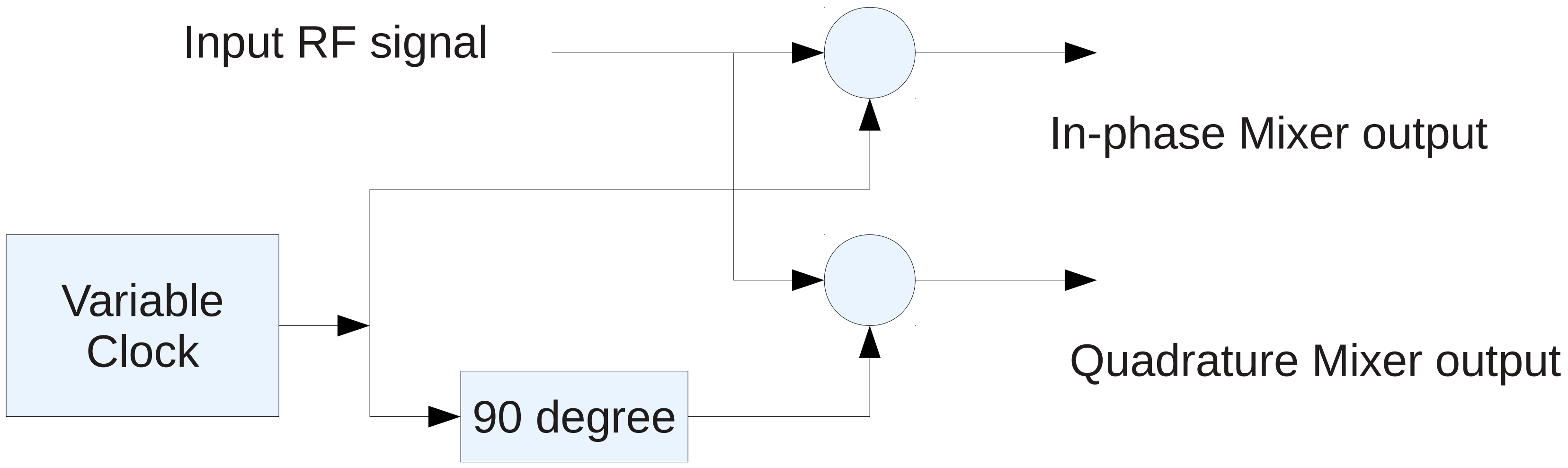
This presentation describes the simulation of a Quadrature (I/Q) Mixer using the WaveformViewer feature in eightolives' Workspaces Desktop.

The design was created using eightolives' Schematic with a VHDL export to Workspaces' DesignTool. The design was made simulatable and then exercised using the WavefomViewer.

The purpose of the simulation is to validate intended digital clocking waveforms and observe that inputs are sampled correctly.

Background

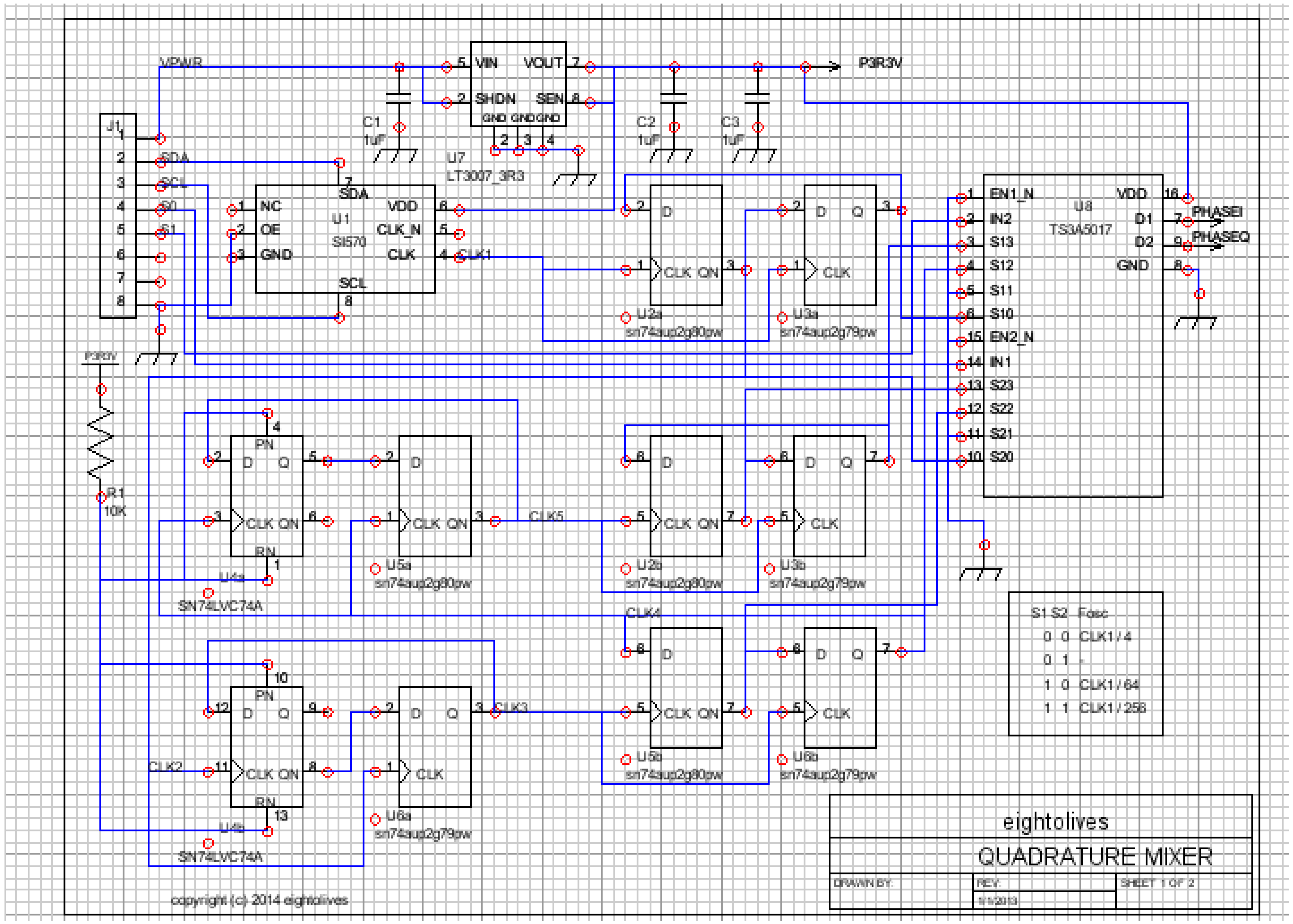
- A Quadrature Mixer is a building block for radios. Sampling radio signals with two waveforms 90 degrees out of phase allows further processing elements to eliminate unwanted mixer products.



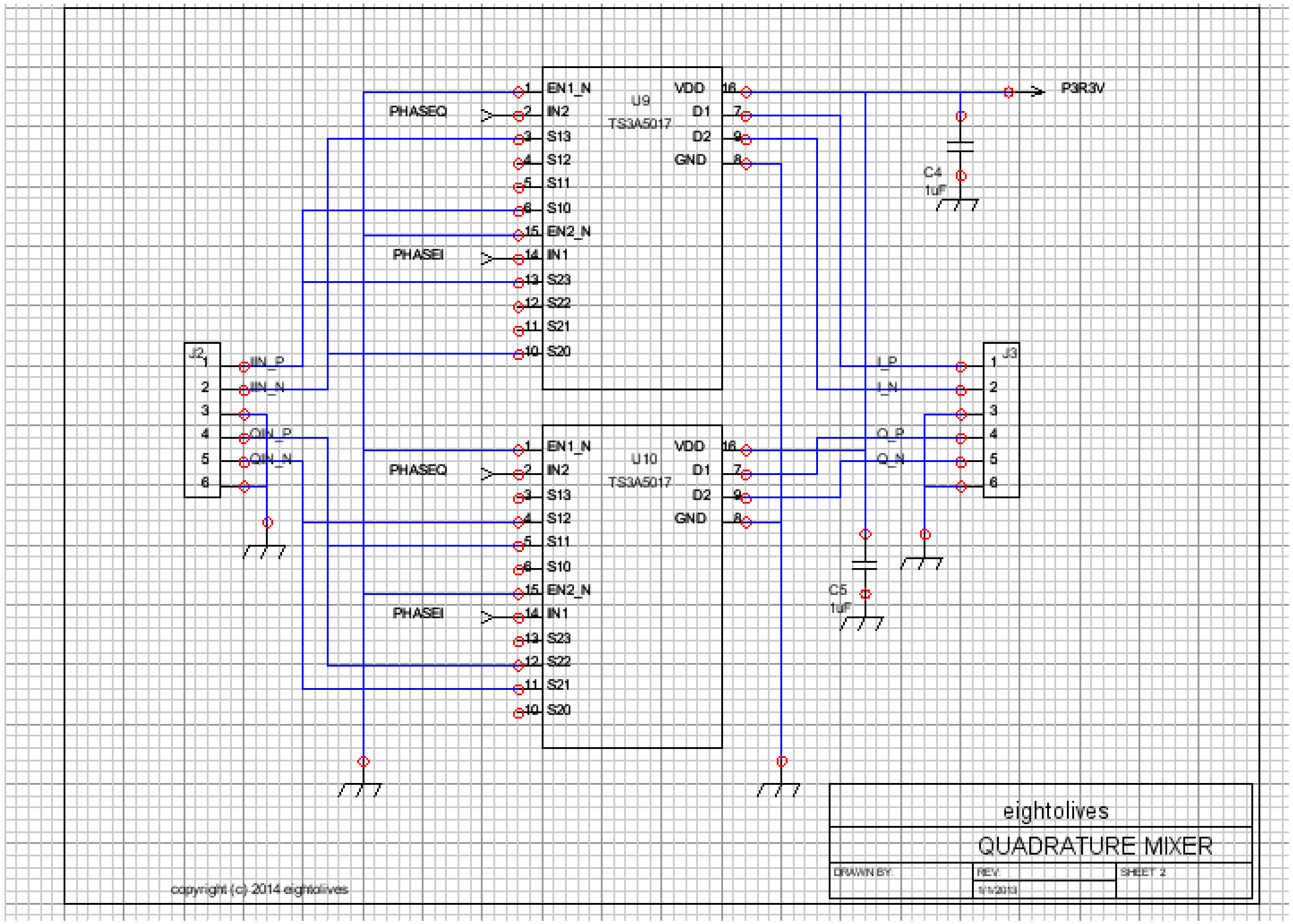
Design Description

- The circuit uses a Silicon Labs Si570 Programmable Oscillator to generate the basic clock. D flip-flops are used to create the I and Q clocks in three different frequency ranges.
- Texas Instruments TS3A5017 Dual 4 to 1 analog selectors are used to select frequency range and sample the I and Q channel inputs.
- Outputs are not filtered

Schematic Sheet 1: Clock Generation

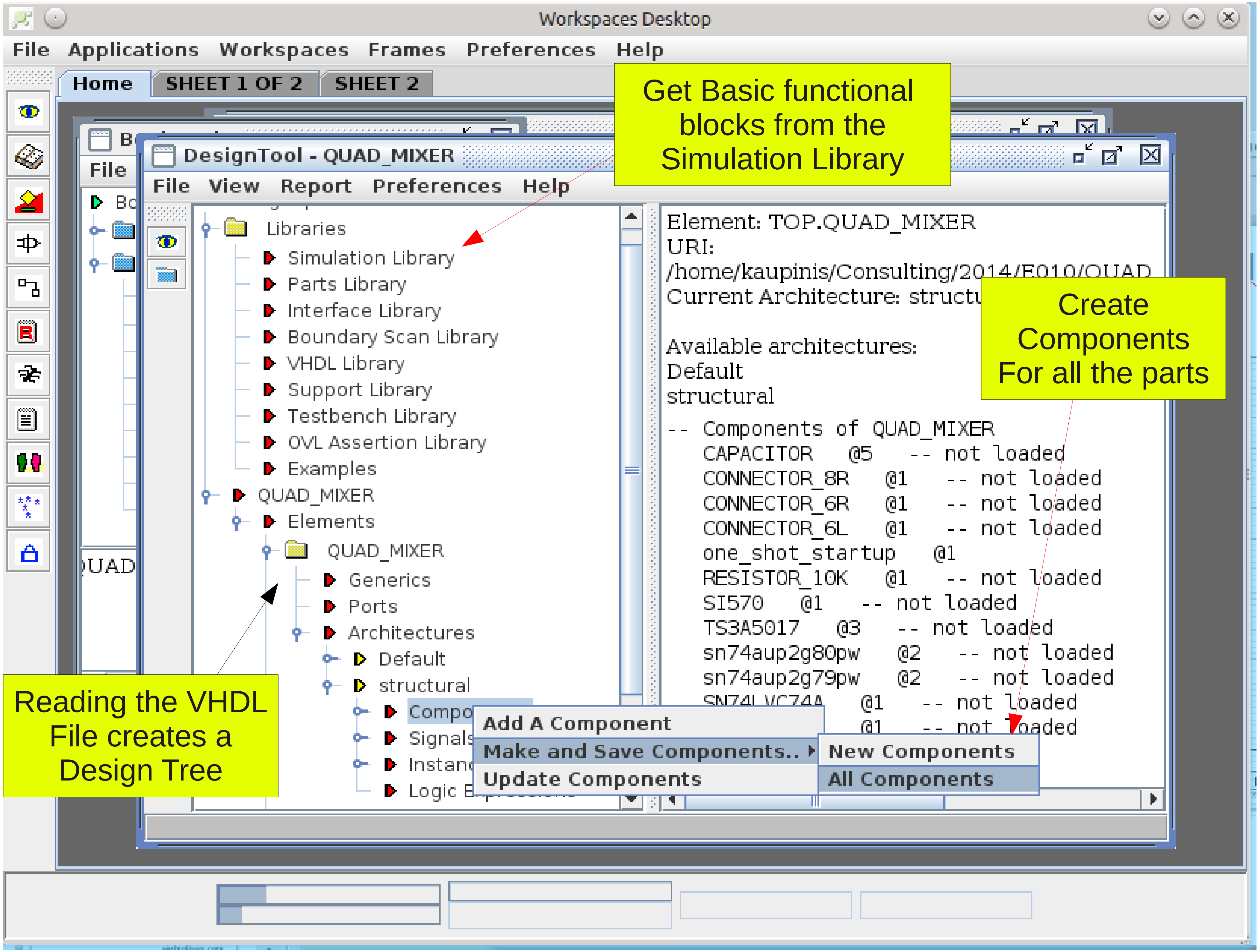


Schematic Sheet 2: Switching Mixers



Getting to a simulation

- The schematic is exported to a VHDL file (menu option *Design > Generate VHDL*) (*File > Save As..*) which can be input and edited as a design tree in Workspaces' DesignTool.
- Empty models for each component are created from the Components folder menu in the design tree (*Make and Save Components > All Components*)
    - Components not participating in simulation (caps, connectors, voltage regulator, etc) need to have the attribute “PRIMITIVE” added and set to “true”
    - Components participating in the simulation need functionality added.



Get Basic functional blocks from the Simulation Library

Create Components For all the parts

Reading the VHDL File creates a Design Tree

```
Element: TOP.QUAD_MIXER
URI:
/home/kaupinis/Consulting/2014/F010/QUAD
Current Architecture: structu

Available architectures:
Default
structural

-- Components of QUAD_MIXER
   CAPACITOR    @5    -- not loaded
   CONNECTOR_8R    @1    -- not loaded
   CONNECTOR_6R    @1    -- not loaded
   CONNECTOR_6L    @1    -- not loaded
   one_shot_startup    @1
   RESISTOR_10K    @1    -- not loaded
   SI570    @1    -- not loaded
   TS3A5017    @3    -- not loaded
   sn74aup2g80pw    @2    -- not loaded
   sn74aup2g79pw    @2    -- not loaded
   SN74LVC74A    @1    -- not loaded
                 @1    -- not loaded
```

Adding Functionality to Models

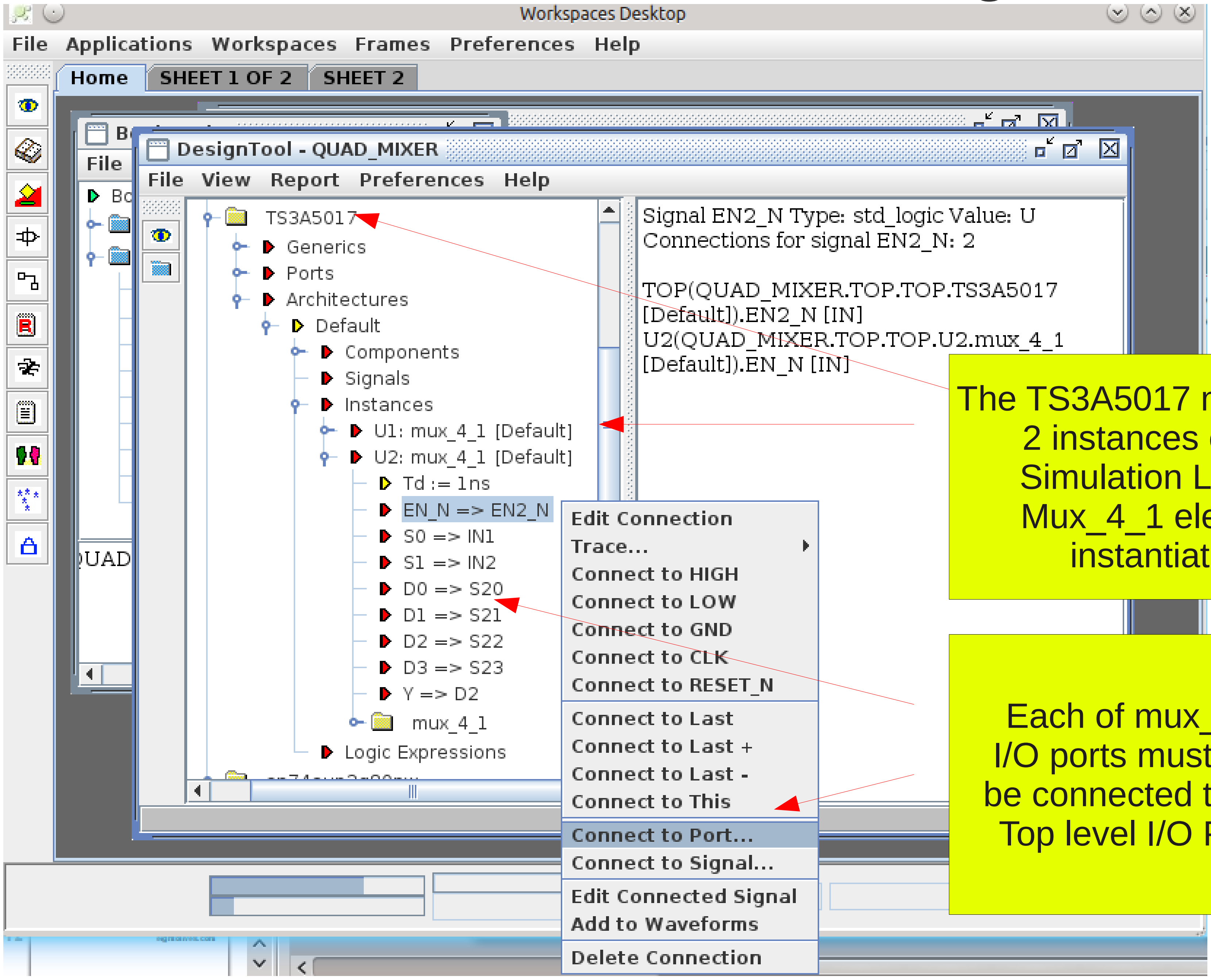
- Unfortunately, the current VHDL parser (version 1) doesn't support functionality models in VHDL
- You can create and use your own functional models in either Java or Javascript starting with templates created from DesignTool (separate presentations and demos explain how) or
- You can select basic functional building blocks from the eightolives Simulation Library and add them to the components.

Simulation Library Building Blocks

- The Simulation Library contains simulatable Java models of basic Elements that can be loaded, instantiated and connected in the DesignTool or in the VHDL files.
- The library includes, basic logic gates (and, nand, or, nor, xor), flip-flops, counters, adders, decoders, multiplexes, RAM, one-shots, clock generators, boundary scan cells and special logic functions.

Simulation Library Elements Used for this design...

- The *clock* Simulation Library element was instantiated in the Si570 clock component
- Two instances of the *dff* element were instantiated in each of the three, dual flip flop component types used
- Two instances of the *mux_4_1* element was instantiated in the TS3A5017 analog multiplexer.
- A *one_shot_startup* element was instantiated in the top level VHDL file to create a power-on reset pulse needed for simulation only
  - The one-shot was connected to the 3.3 Volt power signal P3R3V which connects to all the components.



```
Signal EN2_N Type: std_logic Value: U
Connections for signal EN2_N: 2

TOP(QUAD_MIXER.TOP.TOP.TS3A5017
[Default]).EN2_N [IN]
U2(QUAD_MIXER.TOP.TOP.U2.mux_4_1
[Default]).EN_N [IN]
```

The TS3A5017 model has 2 instances of the Simulation Library Mux_4_1 element instantiated

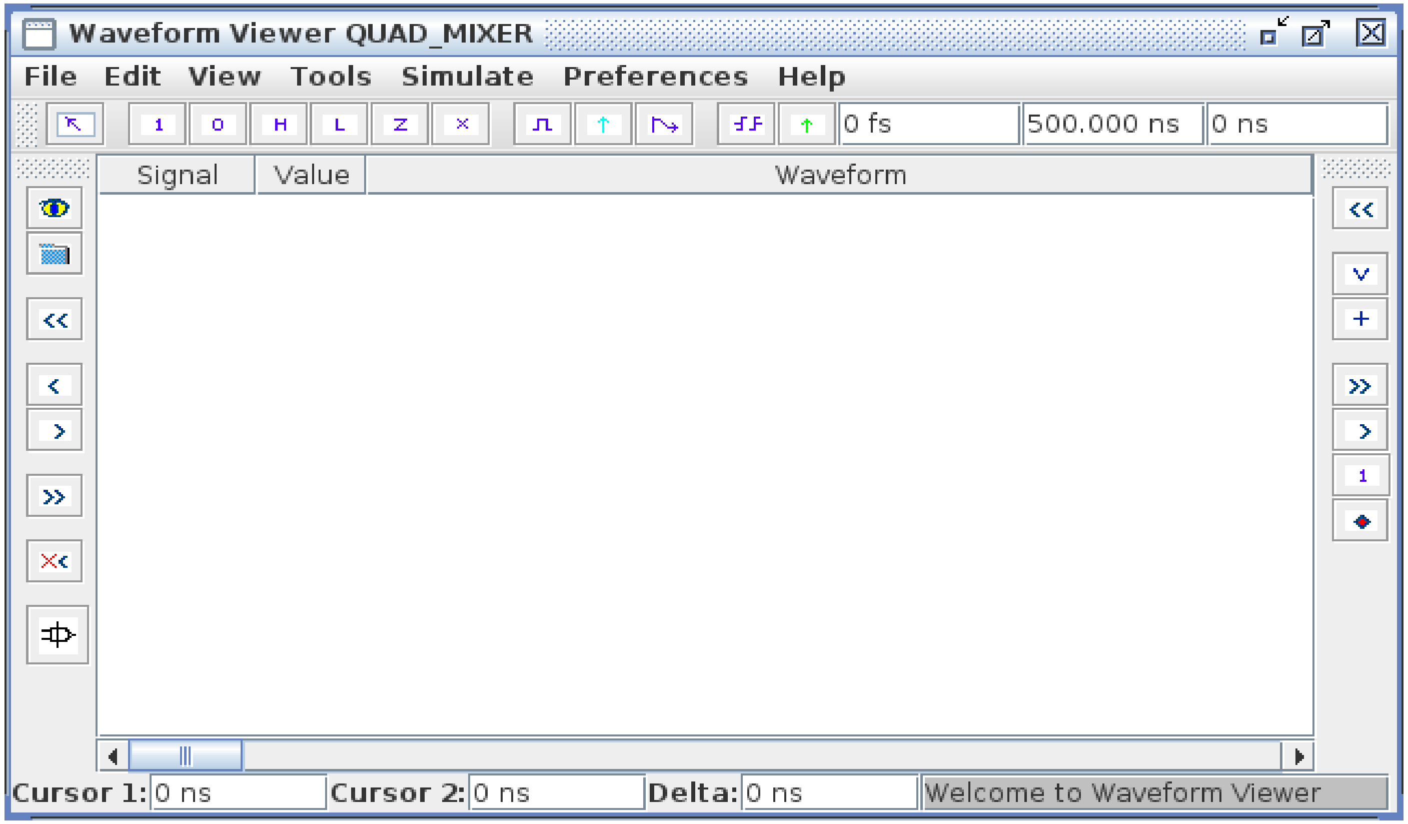
Each of mux_4_1 I/O ports must then be connected to the Top level I/O Ports

Starting the WaveformViewer

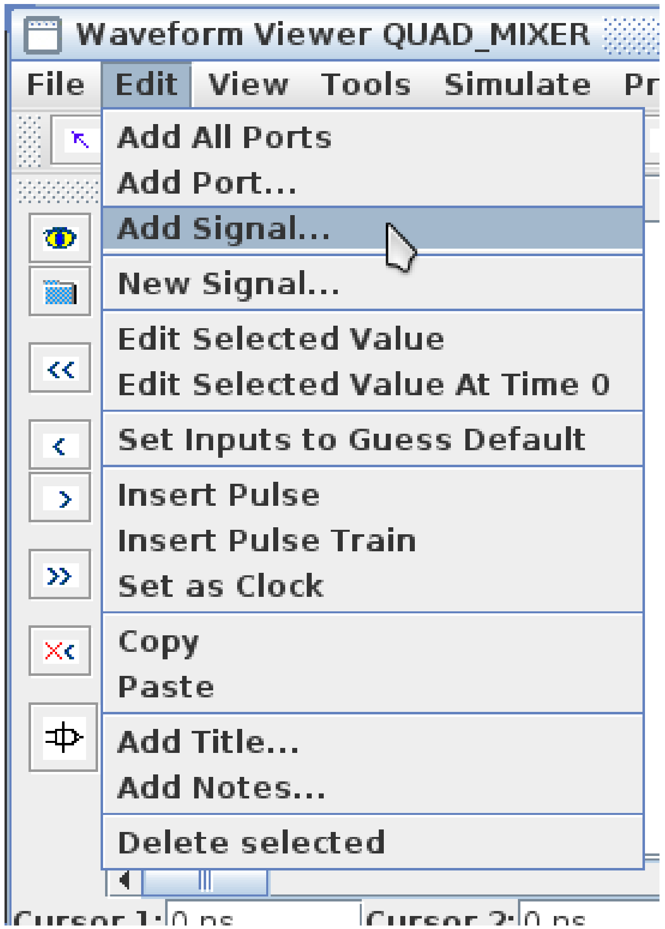
- To make all the models consistent (or “synced”), right click “Elements” and select menu option *Update All To Library*
- Right-click QUAD_MIXER and select *Ops* > *Update Instances To Library*
- Then right click QUAD_MIXER and select *Check* > *Simulatable*
- Right-click QUAD_MIXER and select *View* > *Waveforms*

WaveformViewer

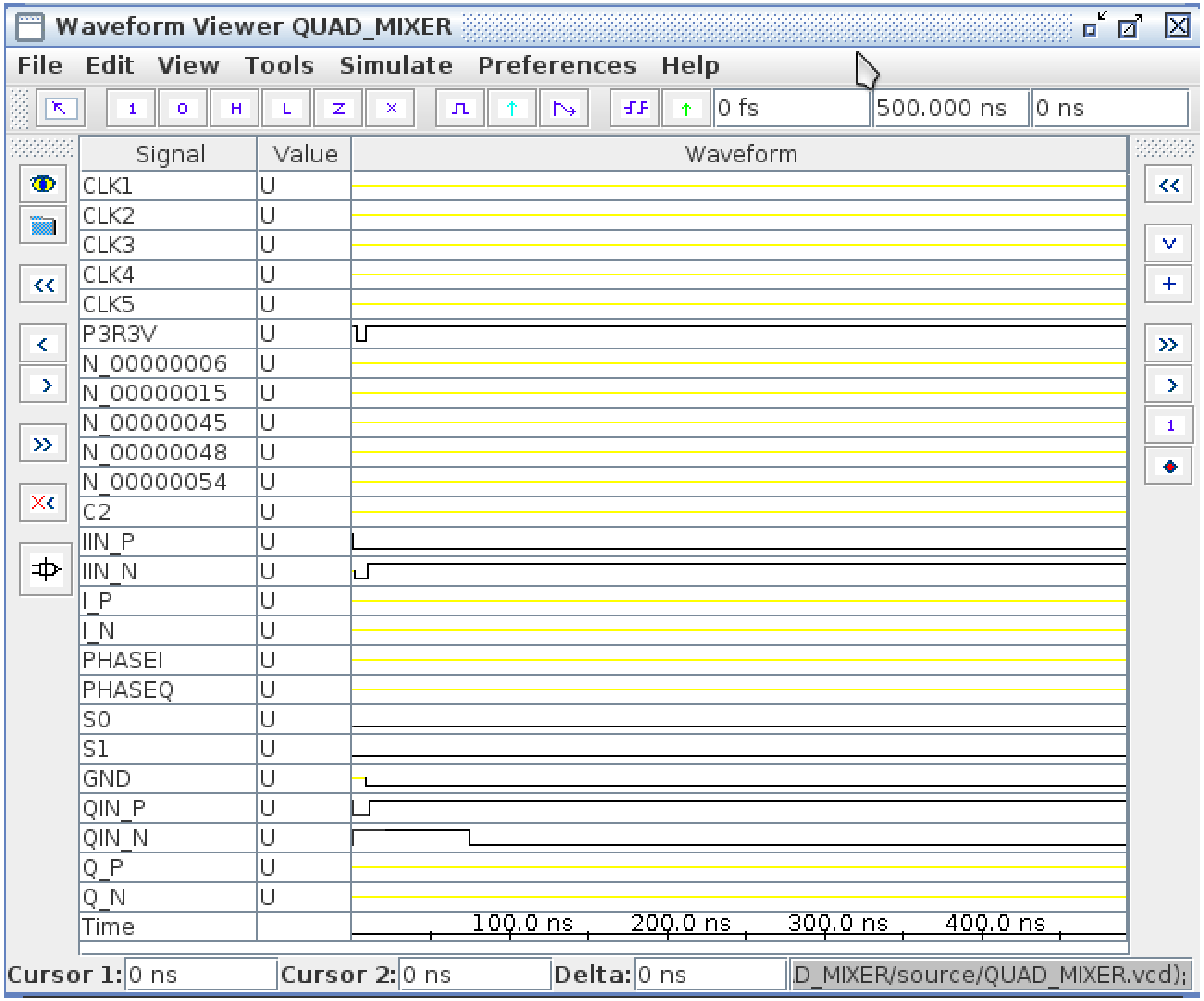
Zoom out
Scroll left
Scroll right
Zoom in


Waveform Viewer QUAD_MIXER
File Edit View Tools Simulate Preferences Help
1 0 H L Z X
0 fs
500.000 ns
0 ns
Signal
Value
Waveform
Cursor 1: 0 ns
Cursor 2: 0 ns
Delta: 0 ns
Welcome to Waveform Viewer

Restart
Load VCD File
Add to Queue
Run
Run For...
Single Step
Stop



- You can add wavefoms to the viewer using the menus
- You can add wavefoms to the viewer from the design tree
- File > Save As > .vcd file to save and use your settings again
- You can also “draw waveforms” for stimulus and save that in the .vcd file



The simulation sequence is:

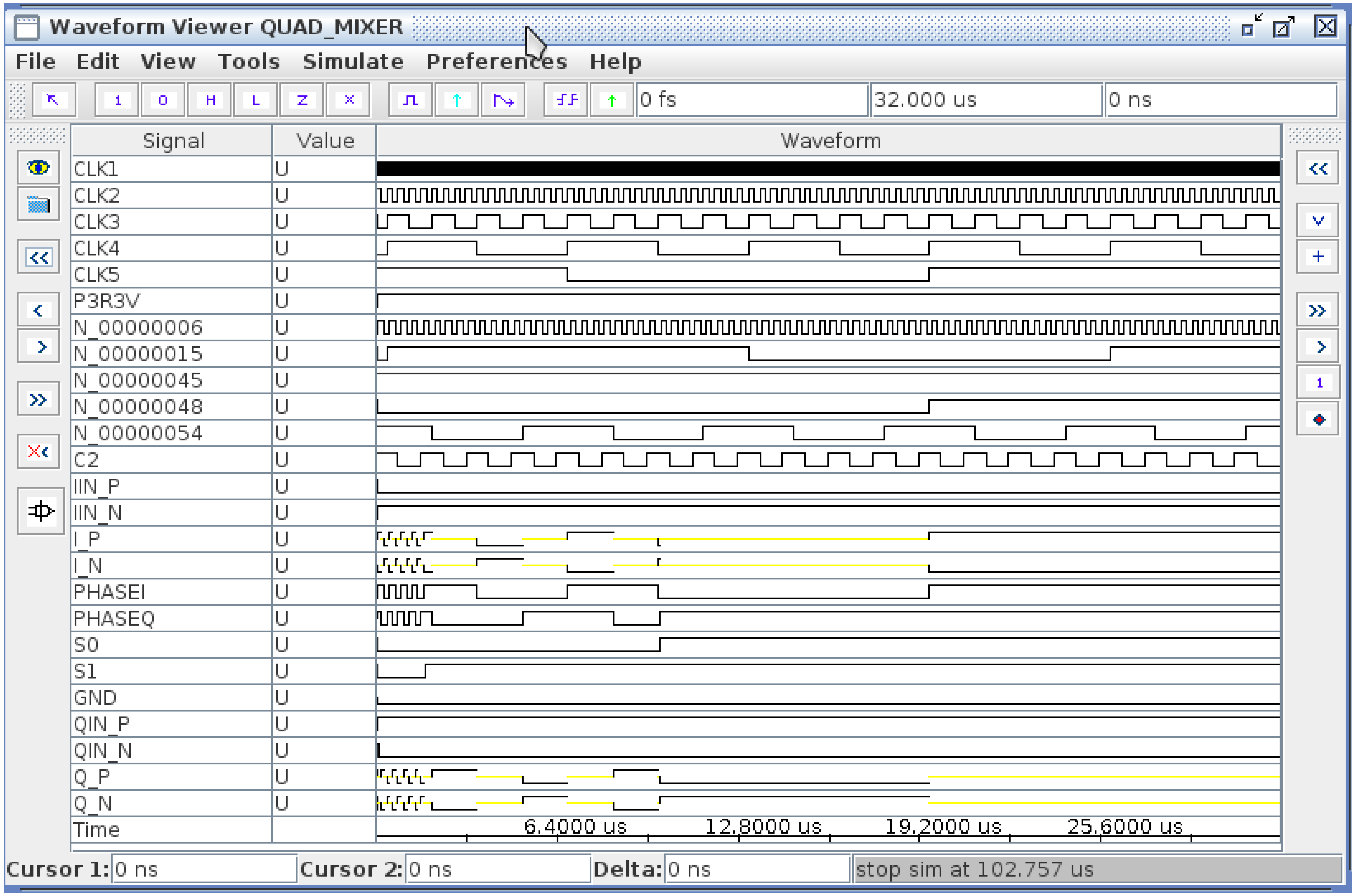
1. RESTART

2. Load VCD File

3. Add to Sim

4. Run

This simulation does not automatically stop, so you must click STOP after ~100 us



Waveform Viewer QUAD_MIXER

0 fs | 32.000 us | 0 ns

Signal	Value
CLK1	U
CLK2	U
CLK3	U
CLK4	U
CLK5	U
P3R3V	U
N_00000006	U
N_00000015	U
N_00000045	U
N_00000048	U
N_00000054	U
C2	U
IIN_P	U
IIN_N	U
I_P	U
I_N	U
PHASEI	U
PHASEQ	U
S0	U
S1	U
GND	U
QIN_P	U
QIN_N	U
Q_P	U
Q_N	U
Time	

Waveform

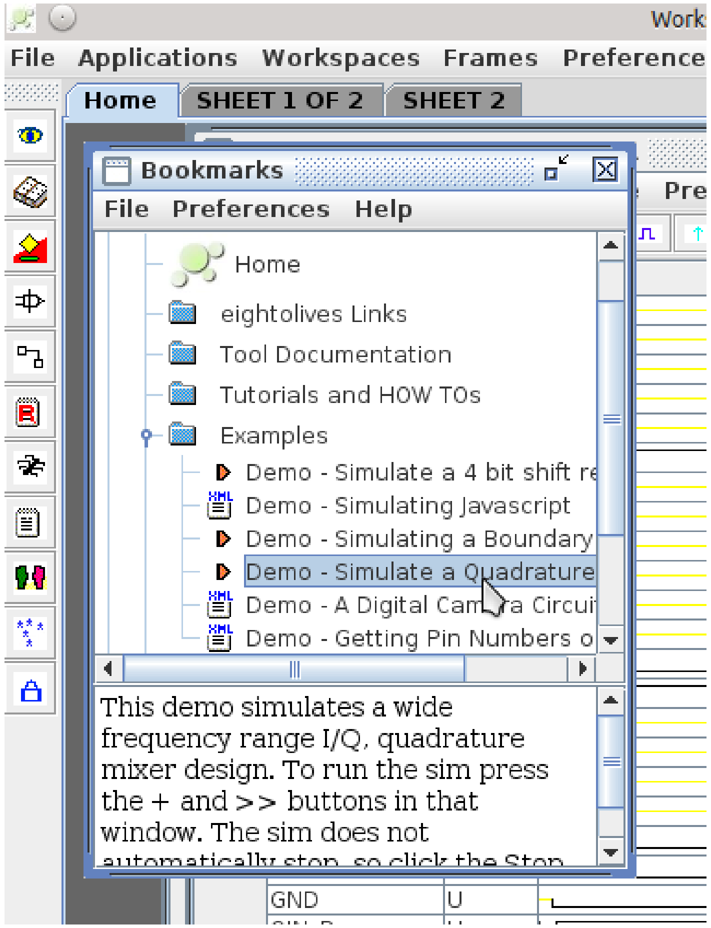
6.4000 us 12.8000 us 19.2000 us 25.6000 us

Cursor 1: 0 ns Cursor 2: 0 ns Delta: 0 ns stop sim at 102.757 us

Results

- The simulation found a mis-wiring in the original schematic.
- It shows that the clocks for the 3 frequency bands have the correct phase relation.
- It shows the mixer outputs behaving as expected.

You can click to run this simulation


Work
File Applications Workspaces Frames Preference
Home
SHEET 1 OF 2
SHEET 2
Bookmarks
File Preferences Help
Home
eightolives Links
Tool Documentation
Tutorials and HOW TOs
Examples
Demo - Simulate a 4 bit shift re
Demo - Simulating Javascript
Demo - Simulating a Boundary
Demo - Simulate a Quadrature
Demo - A Digital Camera Circui
Demo - Getting Pin Numbers o
Pre
GND
U

This demo simulates a wide frequency range I/Q, quadrature mixer design. To run the sim press the + and >> buttons in that window. The sim does not automatically stop, so click the Stop

- You can load and run this demo from the Bookmarks tool
- Select Resources > Examples > Demo – Simulate A Quadrature Mixer

For more information

- Check the tutorials at: http://www.eightolives.com/tutorials.htm
  - Using eightolives' Schematic
  - Workspaces Desktop Tool Overview
  - Modeling Hardware in Java
  - Simulating Javascript Models
- Try the other simulation examples
- Read the Workspaces Desktop Users Manual
- Consult the com.eightolives.Hardware API