Simulating Schematics With Modelsim

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Abstract

The MentorGraphics Modelsim simulator is a world class VHDL simulator that can be used to simulate printed circuit board designs.

Schematics generated using the MentorGraphics' Design Architect tool can be exported to VHDL.

Workspaces Desktop tools can help reduce the time migrating from schematics to simulation.

Why Simulate?

Module level digital simulation is useful to:

- Verify module internal interconnect
- Verify function and interaction of the various components
- Verify coarse timing
- Generate test vectors
- Support integration problem resolution

Create a Module Schematic

- A schematic is a graphical representation of components and interconnect
- It is used to convey an electrical module design concept to physical implementers
- Creating a schematic is an engineering specialty - part science and part art
- To be useful for simulation, a schematic made with Design Architect (DA) needs to meet certain requirements

Migrating Schematics to Sim

- Create and use a copy of the schematic using Design Manager in order to preserve symbolic links. Always work on a copy!
- The DA menu command Check > Schematic must PASS before Exporting VHDL will succeed
- Certain rules regarding properties and labeling must be enforced to create a useful VHDL file
  - Using a dofile script, such as fix_schematic, is useful to automate rule enforcement

The Rules

- Any schematic item whose REF property starts with J or P or is considered a PORT should be assigned a property of CLASS = P (that puts it on the VHDL entity as a Port)
- All REF properties should be copied to INST (the INST property is used as the label for instantiated VHDL parts)
- REFS with U, J, P, AR and L should be unique (i.e. not duplicated)
- A non-homogeneous component (such as a large pin count device with it's symbol drawn in several pieces) should have each piece uniquely labeled such as U1_A, U1_B etc.

Sandbox

- We recommend constructing a “Sandbox” directory structure from which you do your simulation
- See “All About Sandboxes” to learn how you easily create one using Workspaces Desktop

Making the VHDL Files

- Once the rules are enforced and Check Schematic passes, use the DA menu option File > Export VHDL
- For Component Viewpoint: select your design
- For Output to Path: make a directory “vhdl_write” in your sandbox or project directory and specify that path
- Modify Options: select Configuration in File
- Then click OK

Now we must post-process the files

- Exporting VHDL from Design Architect produces the design's entity file, separate architecture file, configuration file, global file and .vxt file
- Now we want to:
  - Combine entity and architecture
  - Make substitutions for all alias declarations
  - Combine non-homogeneous symbols (typically FPGAs, CPLDs)
  - Generate VHDL “wrappers” or “shells” for each component type
  - Update configuration particularly to specify functionality of Rs and Cs
  - Generate scripts
  - Compile and correct errors
- We can use the Workspaces Desktop DesignTool to do some of the steps

Create a New VHDL file for the Design

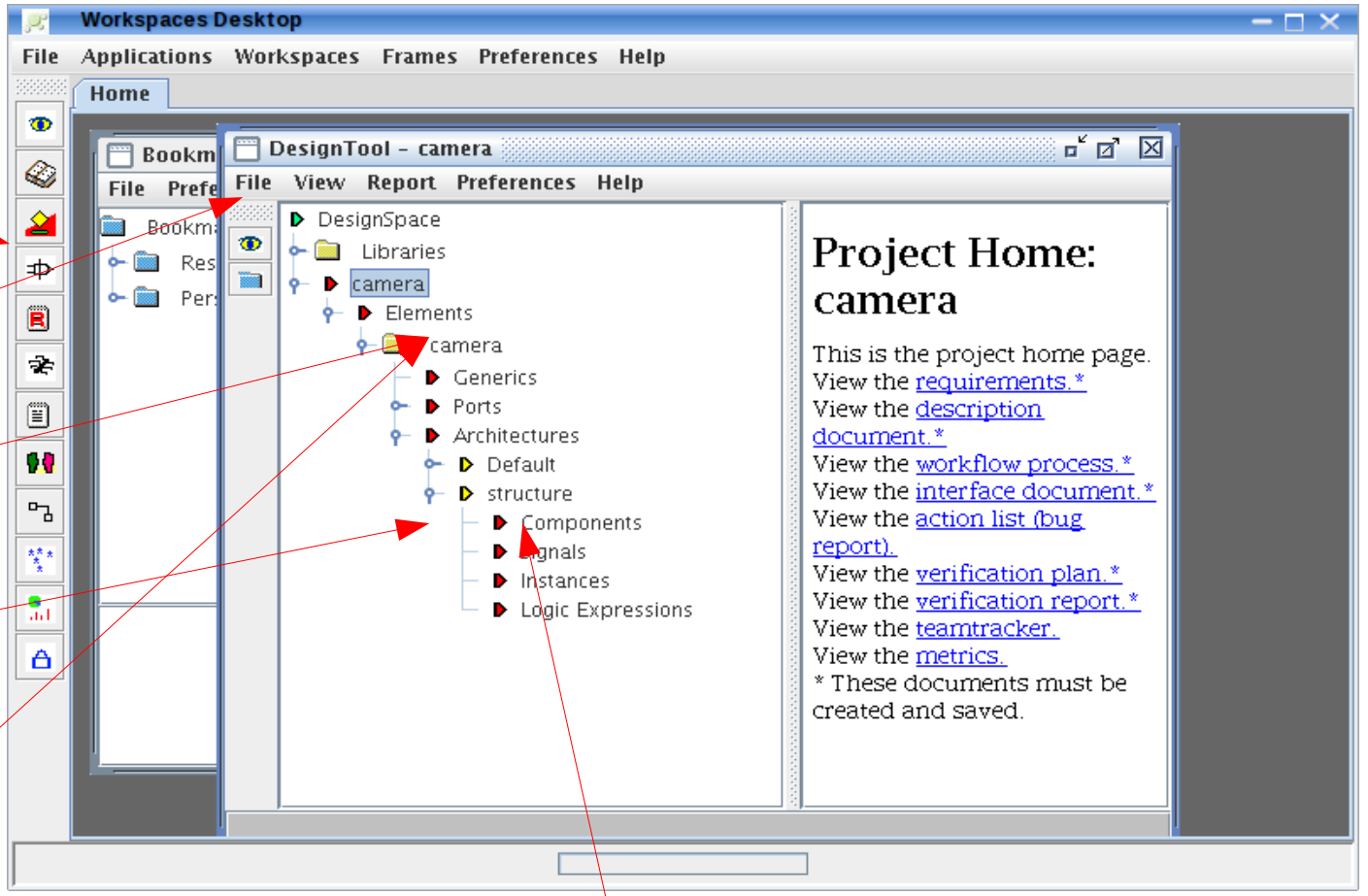
Click gate icon to Invoke tool

Import the entity file

Right click the entity Element and select Import Architecture

Right click structure and select Merge Non-Homogeneous Components

Right click on element and Make New VHDL. Then save the file in your source directory Select Make Testbench And save in testbench Directory.



Right click structure and select Make Configuration for Testbench, Make Compile Script Make Simulation Script and Make Testbench / Config Compile Script. Save all these in sim

Modeling the Components

- To create VHDL shells (wrappers) for all the components used, right click Components and select Make and Save Components > All Components
- The resulting VHDL files have “empty” architectures for which you need to get models if the component is an active participant of the simulation

Ready to compile

- At this point the design should compile correctly by executing the compile script in the sandbox's sim directory.
- If not, this is the time to debug items until it does compile
- Since we have not included functionality for the components, it won't do anything in sim yet

Adding Models

- Where do VHDL simulation models come from?
  - Use your own FPGA and CPLD code for those parts
  - Use third-party libraries
  - Download models available from free web sites
  - Vendors sometimes provide models (IDT)
  - Use available in-house libraries (reuse)
  - Make your own
- The quality of the models should be consistent with your simulation objectives
- Don’t expect to get picosecond accuracy.
- Do expect to prove out gross functionality, timing.

For more information

- Refer to MentorGraphics documentation on use of Design Architect, Design Manager and Modelsim
- Check the tutorials at: http://www.eightolives.com/tutorials.htm
  - Workspaces Desktop Tool Overview
  - All About Sandboxes
- Checkout the VHDL resources links at: http://www.eightolives.com/technology.htm
- Read the Workspaces Desktop Users Manual